SGM4062
Over-Voltage Protection IC and Li+ Charger Front-End Protection IC with LDO Mode

GENERAL DESCRIPTION

The SGM4062 is a charger front-end integrated circuit designed to provide protection to Li-Ion batteries from failures of the charging circuitry. The IC continuously monitors the input voltage and the battery voltage. The device operates like a linear regulator, maintaining a 5.1V output with input voltages up to the input over-voltage threshold (V_{OVP} = 6.8V). During input over-voltage conditions, the IC immediately turns off the internal pass FET disconnecting the charging circuitry from the damaging input source. Additionally, if the battery voltage rises to unsafe levels while charging, power is removed from the system. The IC also monitors its die temperature and switches off if it exceeds 145℃. When the IC is controlled by a processor, the IC provides status information about fault conditions to the host.

The SGM4062 is available in Green TDFN-2×2-8L and MSOP-8 (Exposed Pad) packages and is rated over the -40℃ to +85℃ temperature range.

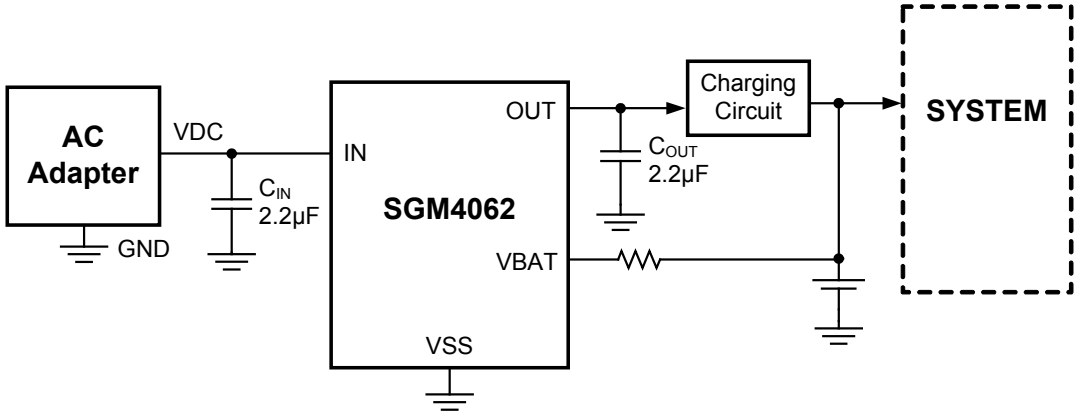
FEATURES

- **Input Over-Voltage Protection**
- **Accurate Battery Over-Voltage Protection**
- **Soft-Start to Prevent Inrush Currents**
- **Soft-Stop to Prevent Voltage Spikes**
- **18V Maximum Input Voltage**
- **Supports up to 1.5A Load Current**
- **Thermal Shutdown**
- **Enable Function**
- **Fault Status Indication**
- **Available in Green MSOP-8 (Exposed Pad) and TDFN-2×2-8L Packages**

APPLICATIONS

Smart Phones, Mobile Phones
PDAs
MP3 Players
Low-Power Handheld Devices

APPLICATION SCHEMATIC



PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
SGM4062	TDFN-2×2-8L	-40℃ to +85℃	SGM4062YDE8G/TR	4062 XXXX	Tape and Reel, 3000
	MSOP-8 (Exposed Pad)	-40℃ to +85℃	SGM4062YPMS8G/TR	SGM4062 YPMS8 XXXXX	Tape and Reel, 3000

NOTE: XXXX = Date Code. XXXXX = Date Code and Vendor Code.

Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

ABSOLUTE MAXIMUM RATINGS

IN (with respect to VSS)..... -0.3V to 28V
OUT (with respect to VSS)..... -0.3V to MIN (V_{IN} + 0.3V, 6V)
$\overline{FAULT}$, $\overline{CE}$, VBAT (with respect to VSS)
..... -0.3V to 6V
Output Source Current (OUT Pin)..... 2A
Output Sink Current ($\overline{FAULT}$ Pin)..... 15mA
Package Thermal Resistance
TDFN-2×2-8L, θ_{JA}..... 75℃/W
MSOP-8 (Exposed Pad), θ_{JA}..... 140℃/W
Junction Temperature.....+150℃
Storage Temperature Range .....-65℃ to +150℃
Lead Temperature (Soldering 10 sec) .....+260℃
ESD Susceptibility
HBM (SGM4062YPMS8G) 3000V
HBM (SGM4062YDE8G) 4000V
MM.....200V

RECOMMENDED OPERATING CONDITIONS

Operating Temperature Range .....-40℃ to +85℃
IN Voltage Range, V_I .....3.3V to 18V
Current, OUT Pin, I_O .....1.5A (MAX)

OVERSTRESS CAUTION

Stresses beyond those listed may cause permanent damage to the device. Functional operation of the device at these or any other conditions beyond those indicated in the operational section of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ESD SENSITIVITY CAUTION

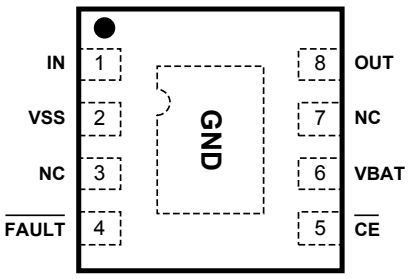
This integrated circuit can be damaged by ESD if you don't pay attention to ESD protection. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, specification or other related things if necessary without notice at any time.

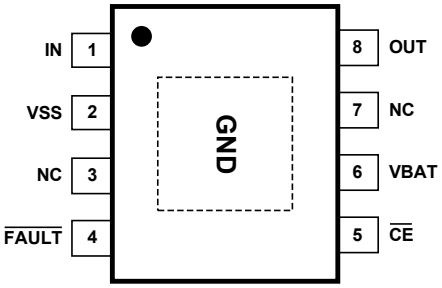
PIN CONFIGURATION

(TOP VIEW)



TDFN-2×2-8L

(TOP VIEW)



MSOP-8 (Exposed Pad)

PIN DESCRIPTION

PIN	NAME	FUNCTION
1	IN	Input Power. Connected to external DC supply. Bypass IN to VSS with a ceramic capacitor (1μF MIN).
2	VSS	Ground Terminal. Connect to the thermal pad and to the ground rail of the circuit.
3, 7	NC	Do not Connect to Any External Circuit.
4	$\overline{\text{FAULT}}$	Open-Drain Device Status Output. $\overline{\text{FAULT}}$ is pulled to VSS internally when the input pass FET has been turned off due to input over-voltage, an over-temperature condition, or because the battery voltage is outside safe limits. $\overline{\text{FAULT}}$ is high impedance during normal operation.
5	$\overline{\text{CE}}$	Active-Low Chip Enable Input. Connect $\overline{\text{CE}}$ = “HIGH” to turn the input pass FET off. Connect $\overline{\text{CE}}$ = “LOW” to turn the internal pass FET on, connecting the input to the charging circuitry. $\overline{\text{CE}}$ is internally pulled down and pull-down resistor is about 200kΩ.
6	VBAT	Battery Voltage Sense Input. Connected to pack positive terminal through a 10kΩ resistor.
8	OUT	Output Terminal to the Charging System. Bypass OUT to VSS with a ceramic capacitor (2.2μF MIN).
Exposed Pad	GND	The Thermal Pad is Electrically Connected to VSS Internally. The thermal pad must be connected to the same potential as the VSS pin on the printed circuit board. Do not use the thermal pad as the primary ground input for the device. VSS pin must be connected to ground at all times.

ELECTRICAL CHARACTERISTICS

(T_A = +25℃, $\overline{CE}$ = LOW, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
INPUT						
Under-Voltage Lockout, Input Power Detected Threshold	UVLO	V_{IN} = 0V to 3V	2.5	2.65	2.8	V
Hysteresis on UVLO	$V_{hys(UVLO)}$	V_{IN} = 3V to 0V		225		mV
Deglitch Time, Input Power Detected Status	$t_{DGL(PGOOD)}$	Time measured from V_{IN} = 0V to 5V, 1μs rise-time		9		ms
Operating Current	I_{DD}	V_{IN} = 5V, no load on OUT pin		185	260	μA
Standby Current	I_{STDBY}	$\overline{CE}$ = HIGH, V_{IN} = 5.5V		0.5	2	μA
INPUT-TO-OUTPUT CHARACTERISTICS						
Q1 Off-State Leakage Current	I_{OFF}	$\overline{CE}$ = HIGH, V_{IN} = 5.5V			5	μA
Dropout Voltage IN to OUT	V_{DO}	V_{IN} = 5V, I_{OUT} = 0.5A		120	170	mV
INPUT OVER-VOLTAGE PROTECTION						
Output Voltage	$V_{O(REG)}$	V_{IN} = 5.5 to V_{OVP} - $V_{hys(OVP)}$, no load on OUT pin	4.9	5.1	5.3	V
Input Over-Voltage Protection Threshold	V_{OVP}		6.35	6.8	7.05	V
Hysteresis on OVP	$V_{hys(OVP)}$		50	120	280	mV
Input Over-Voltage Protection Propagation Delay (1)	$t_{PD(OVP)}$	V_{IN} = 6V to 9V		200		ns
Recovery Time from Input Over-Voltage Condition	$t_{REC(OVP)}$	Time measured from V_{IN} = 9V to 6V, 1μs fall-time		9		ms
BATTERY OVER-VOLTAGE PROTECTION						
Battery Over-Voltage Protection Threshold	BV_{OVP}	V_{OVP} - $V_{hys(OVP)}$ > V_{IN} > 4.5V	4.275	4.35	4.41	V
Hysteresis on BV_{OVP}	$V_{hys(BVovp)}$	V_{OVP} - $V_{hys(OVP)}$ > V_{IN} > 4.5V	190	255	320	mV
Input Bias Current on VBAT Pin	I_{VBAT}			20	180	nA
Deglitch Time, Battery Over-Voltage Detected	$t_{DGL(BVovp)}$	V_{IN} > 4.5V, time measured from V_{VBAT} rising from 4.1V to 4.5V to $\overline{FAULT}$ going low		180		μs
THERMAL PROTECTION						
Thermal Shutdown Temperature	$T_{J(OFF)}$			145		℃
Thermal Shutdown Hysteresis	$T_{J(OFF-HYS)}$			15		℃
LOGIC LEVELS ON $\overline{CE}$						
Logic LOW Input Voltage	V_{IL}				0.4	V
Logic HIGH Input Voltage	V_{IH}		1.4			V
Input LOW Current	I_{IL}			0.3	1.5	μA
Input HIGH Current	I_{IH}	$V_{\overline{CE}}$ = 1.8V		9	15	μA
LOGIC LEVELS ON $\overline{FAULT}$						
Output LOW Voltage	V_{OL}	I_{SINK} = 5mA		0.14	0.3	V
Off-State Leakage Current, HI-Z	I_{lkg}	$V_{\overline{FAULT}}$ = 5V		0.01	25	μA

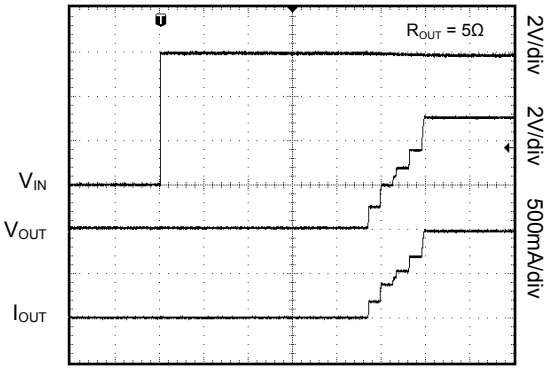
NOTE:

1. Not tested. Specified by design.

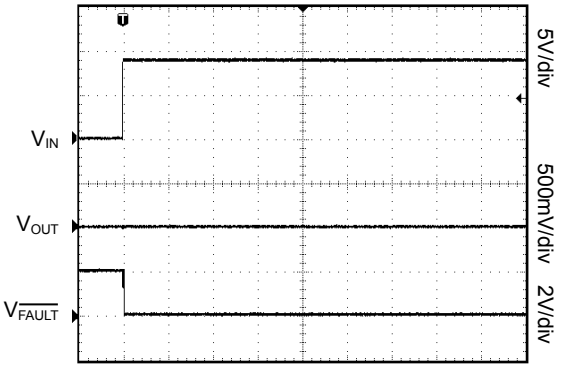
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = +25℃, C_{IN} = C_{OUT} = 2.2μF, unless otherwise noted.

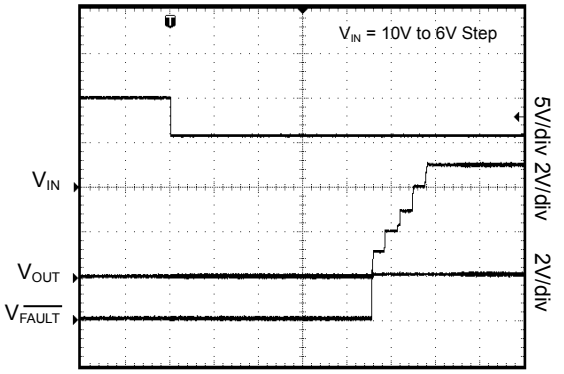
Normal Power-On Showing Soft-Start



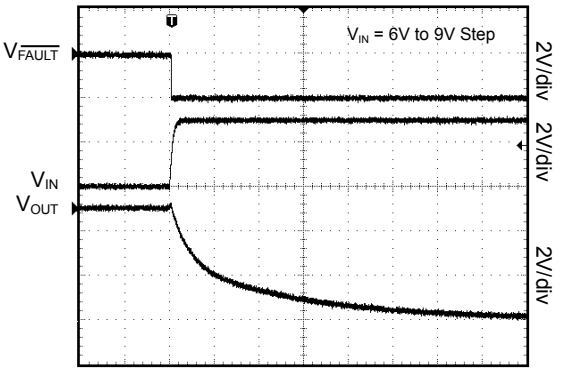
OVP at Power-On



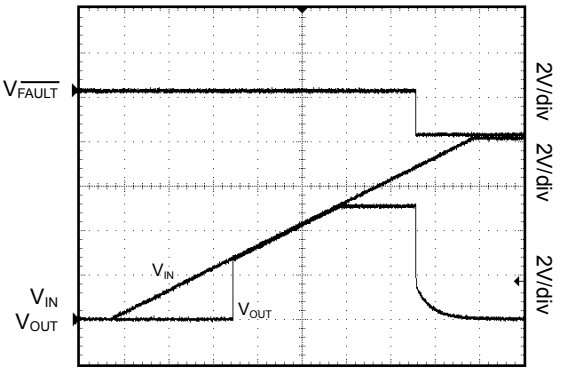
Recovery from OVP



OVP Response for Input Step



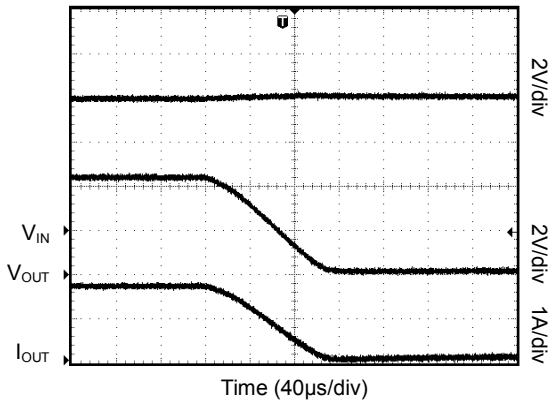
Slow Input Ramp into OVP Event



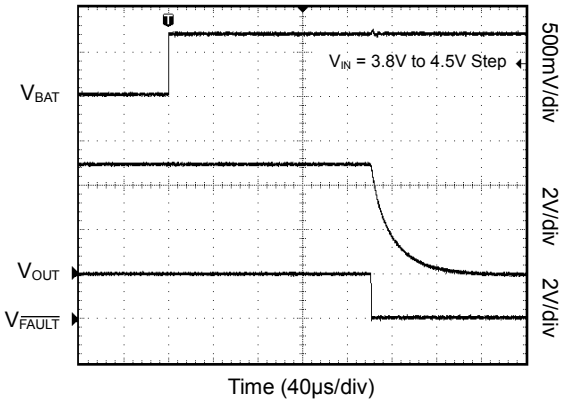
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

T_A = +25℃, C_{IN} = C_{OUT} = 2.2μF, unless otherwise noted.

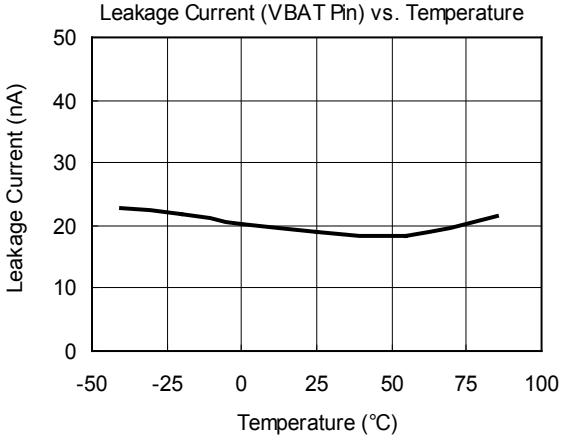
Soft-Stop during OCP Event



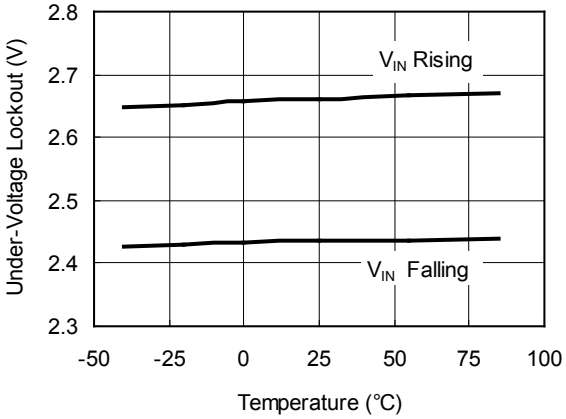
Battery OVP Event



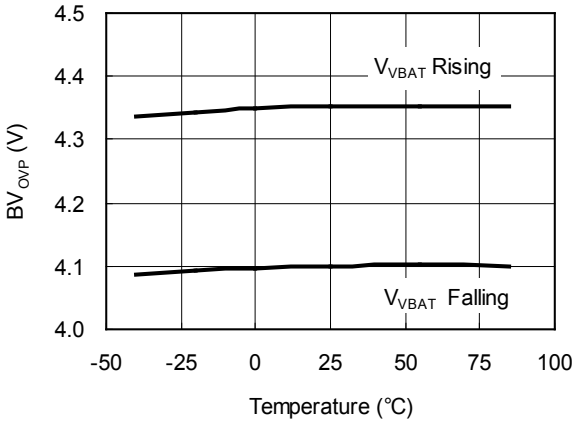
Leakage Current (VBAT Pin) vs. Temperature



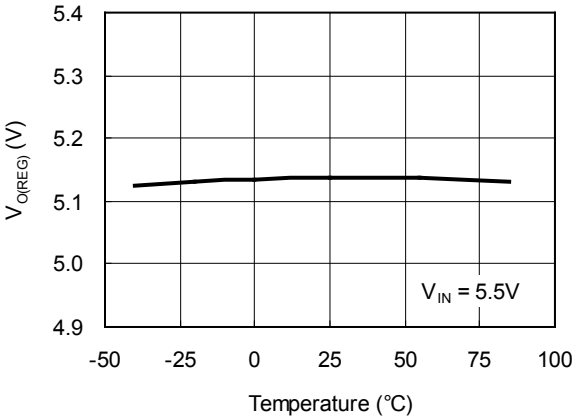
Under-Voltage Lockout vs. Temperature



Battery Over-Voltage Protection Threshold vs. Temperature

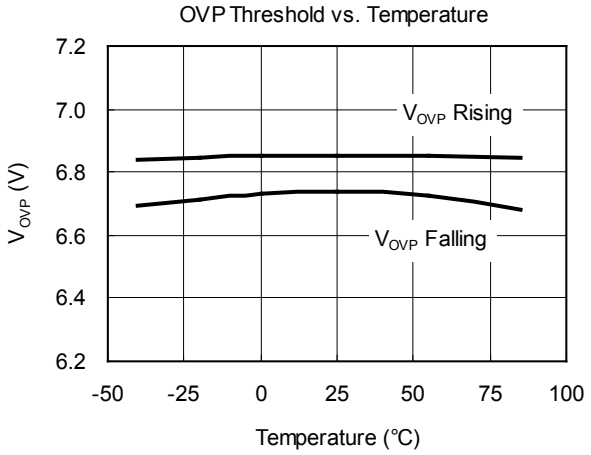


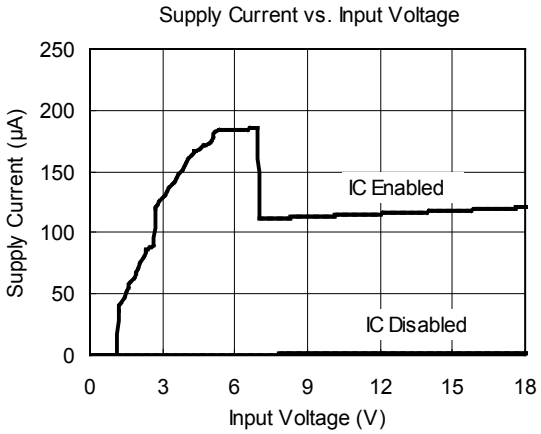
Output Voltage Regulation vs. Temperature



TYPICAL PERFORMANCE CHARACTERISTICS (continued)

T_A = +25℃, C_{IN} = C_{OUT} = 2.2μF, unless otherwise noted.





TYPICAL APPLICATION CIRCUIT

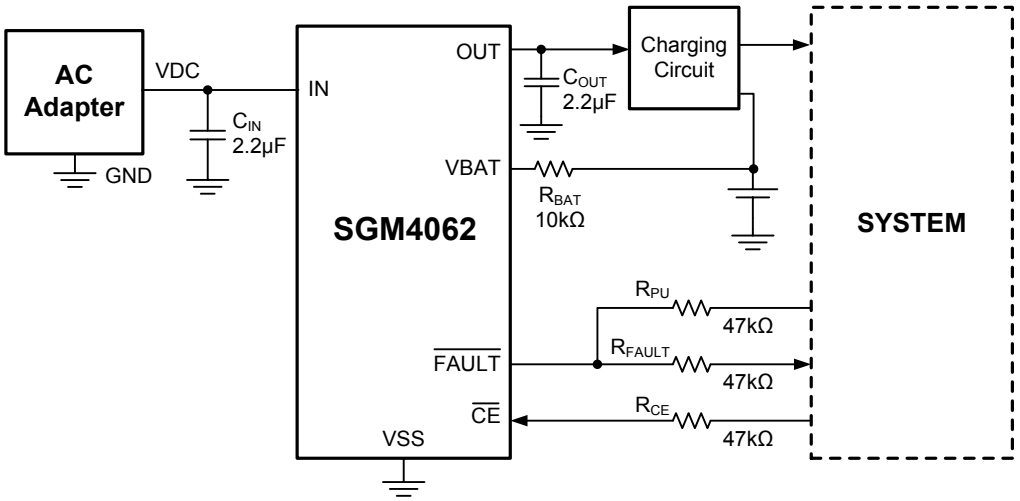


Figure 1. Typical Application Circuit

FUNCTIONAL BLOCK DIAGRAM

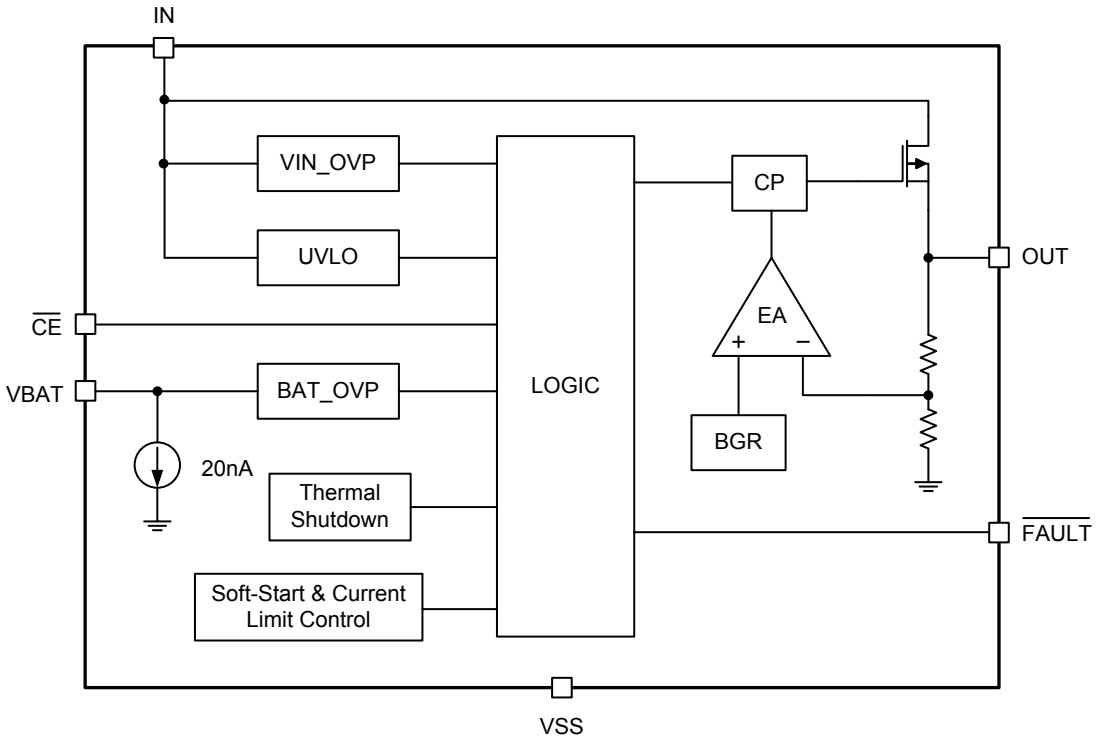
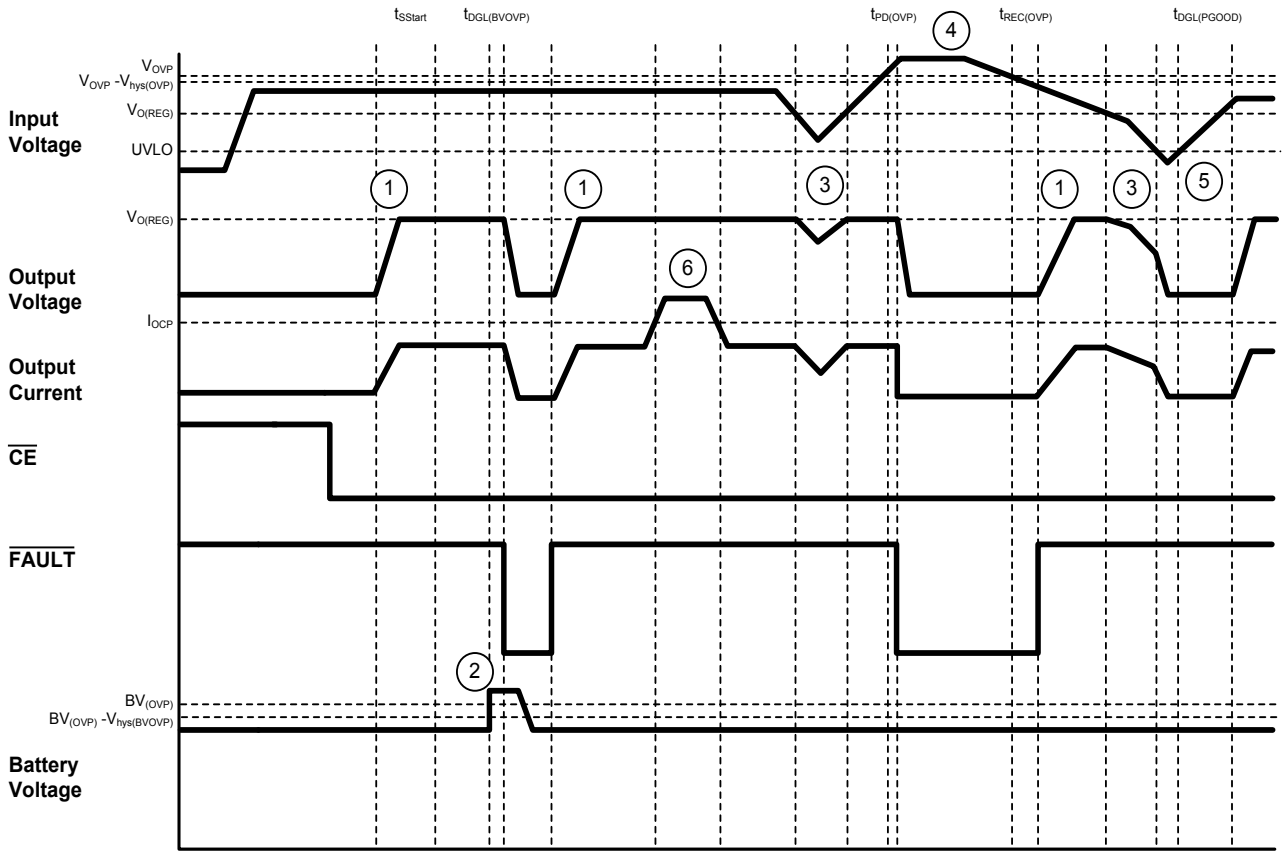


Figure 2. Functional Block Diagram

TIMING DIAGRAM



1. Normal start-up condition
2. Battery over-voltage event
3. $V_{UVLO} < V_{IN} < V_{O(REG)}$, V_{OUT} tracks V_{IN}
4. Input over-voltage event
5. Input below UVLO
6. High-current event during normal operation

Figure 3. Timing Diagram

DETAILED DESCRIPTION

The SGM4062 is a highly integrated circuit designed to provide protection to Li-Ion batteries from failures of the charging circuit and the input source. The IC continuously monitors the input voltage and the battery voltage. The device operates like a linear regulator, maintaining a 5.1V output with input voltages up to the input over-voltage threshold (V_{OVP} = 6.8V). If the input voltage exceeds V_{OVP}, the IC shuts off the pass FET and disconnects the system from input power. Additionally, if the battery voltage rises above 4.35V, the IC switches off the pass FET, removing the power from the system until the battery voltage falls to safe levels. The IC also monitors its die temperature and switches the pass FET off if it exceeds 145℃.

The IC can be controlled by a processor, and also provides status information about fault conditions to the host.

Power-On

The device resets when the input voltage at the IN pin exceeds the UVLO threshold. During power-on reset, the IC waits for duration $t_{DGL(PGOOD)}$ for the input voltage to stabilize. If, after $t_{DGL(PGOOD)}$, the input voltage and battery voltage are within operation limits, the pass FET is turned on. The IC has a soft-start feature to control the inrush current. The soft-start minimizes the ringing at the input due to the resonant circuit formed by the parasitic inductance of the adapter cable and the input bypass capacitor. During the soft-start time, t_{SStart}, the output current is increased in several steps. Each step is 625μs.

Power-Down

The device remains in power-down mode when the input voltage at the IN pin is below the under-voltage threshold (UVLO) of 2.65V. The FET connected between the IN and OUT pins is off, and the status output, $\overline{FAULT}$, is set to high impedance.

Start-Up Overload Current Protection

During start-up, if the eight soft-start steps are completed and the output current exceeds overload current protection (OCP), the IC initiates an OCP check timer ($t_{CHK(OCP)}$). During this check, the output current is clamped to the OCP threshold (I_{OCP}). If the 5ms $t_{CHK(OCP)}$ timer expires and the output current remains clamped by I_{OCP}, the internal pass FET is turned off using the soft-stop method, $\overline{FAULT}$ is pulled low and the $t_{REC(OCP)}$ timer begins. Once the $t_{REC(OCP)}$ timer expires, $\overline{FAULT}$ becomes high impedance and the soft-start sequence restarts. The device repeats the start/fail sequence until the overload condition is removed. Once the overload condition is removed, the OCP circuitry is disabled and the device enters normal operation. At high temperature this overload current protection during start-up may not be working well.

The device continuously monitors the input voltage and the battery voltage as described in detail below:

Input Over-Voltage Protection

The output voltage at OUT pin of the SGM4062 operates similarly to a linear regulator. While the input voltage is less than $V_{O(REG)}$, and above the UVLO, the output voltage tracks the input voltage (less the drop caused by $R_{DS(on)}$ of the pass FET). When the input voltage is greater than $V_{O(REG)}$ (plus the $R_{DS(on)}$ drop) and less than V_{OVP}, the output voltage is regulated to $V_{O(REG)}$. $V_{O(REG)}$ is 5.1V for the SGM4062. If the input voltage is increased above V_{OVP}, the internal pass FET is turned off, removing power from the charging circuitry connected to OUT. The $\overline{FAULT}$ output is then asserted low. When the input voltage drops below V_{OVP} - $V_{hys(OVP)}$ (but is still above UVLO), the pass FET is turned on after a deglitch time of $t_{REC(OVP)}$. The deglitch time ensures that the input supply has stabilized.

DETAILED DESCRIPTION (continued)

Battery Over-Voltage Protection

The battery over-voltage threshold BV_{OVP} is internally set to 4.35V for the SGM4062. If the battery voltage exceeds the BV_{OVP} threshold for longer than $t_{DGL(BVovp)}$, the pass FET is turned off (using soft-stop), and $\overline{FAULT}$ is asserted low. The pass FET is turned on (using the soft-start sequence) once the battery voltage drops to BV_{OVP} - $V_{hys(BVovp)}$.

Thermal Protection

If the junction temperature of the device exceeds $T_{J(OFF)}$, the pass FET is turned off, and the $\overline{FAULT}$ output is asserted low. The FET is turned on when the junction temperature falls below $T_{J(OFF)}$ - $T_{J(OFF-HYS)}$.

Enable Function

The IC has an enable pin which is used to enable and disable the device. Connect the $\overline{CE}$ pin high to turn off the internal pass FET. Connect the $\overline{CE}$ pin low to turn on the internal pass FET and enter the start-up routine. The $\overline{CE}$ pin has an internal pull-down resistor and can be left unconnected. The $\overline{FAULT}$ pin is high impedance when the $\overline{CE}$ pin is high.

Fault Indication

The $\overline{FAULT}$ pin is an active-low, open-drain output. It is in a high-impedance state when operating conditions are safe, or when the device is disabled by setting $\overline{CE}$ high. With $\overline{CE}$ low, the $\overline{FAULT}$ pin goes low whenever any of these events occurs:

1. Input over-voltage
2. Battery over-voltage
3. IC over-temperature

See Figure 3 for an example of $\overline{FAULT}$ conditions during these events. Connect the $\overline{FAULT}$ pin to the desired logic level voltage rail through a resistor between 1kΩ and 50kΩ.

APPLICATION INFORMATION

Selection of R_{BAT}

It is recommended that the battery not be tied directly to the VBAT pin of the device, as under some failure modes of the IC, the voltage at the IN pin may appear on the VBAT pin. This voltage can be as high as 18V, and applying 18V to the battery may cause failure of the device and can be hazardous. Connecting the VBAT pin through R_{BAT} prevents a large current from flowing into the battery in the event of failure. For safety, R_{BAT} must have a high value. The problem with a large R_{BAT} is that the voltage drops across the resistor because of the VBAT bias current, I_{VBAT}, which causes an error in the BV_{OVP} threshold. This error might be over and above the tolerance on the nominal 4.35V BV_{OVP} threshold.

Choosing R_{BAT} in the range of 10kΩ to 100kΩ is a good compromise. If the IC fails with R_{BAT} equal to 10kΩ, the maximum current flowing into the battery would be (18V - 3V)/10kΩ = 1500μA, which is low enough to be absorbed by the bias currents of the system components. R_{BAT} equal to 10kΩ results in a worst-case voltage drop of $R_{BAT} \times I_{VBAT} \approx 1.7mV$. This is negligible compared to the internal tolerance of 60mV on the BV_{OVP} threshold.

If the Bat-OVP function is not required, the VBAT pin can either be connected to VSS or left floating.

Selection of R_{CE}

The $\overline{CE}$ pin can be used to enable and disable the IC. If host control is not required, the $\overline{CE}$ pin can be tied to ground or left unconnected, permanently enabling the device.

In applications where external control is required, the $\overline{CE}$ pin can be controlled by a host processor. As with the VBAT pin (see previous discussion), the $\overline{CE}$ pin must be connected to the host GPIO pin through as large a resistor as possible. The drop across the resistor is given by $R_{CE} \times I_{IH}$ and the limitation of R_{CE} is calculated by equation:

$$V_{OH} - R_{CE} \times I_{IH} > V_{IH}$$

V_{OH} is the high level output voltage from host I/O.

Selection of Input and Output Bypass Capacitors

The input capacitor C_{IN} in Figure 1 is for decoupling and serves an important purpose. Whenever a step change downwards in the system load current occurs, the inductance of the input cable causes the input voltage to spike up. C_{IN} prevents the input voltage from over-shooting to dangerous levels. It is recommended that a ceramic capacitor of at least 1μF be used at the input of the device. It must be located in close proximity to the IN pin.

C_{OUT} in Figure 1 is also important. During an over-voltage transient, this capacitance limits the output overshoot until the power FET is turned off by the over-voltage protection circuitry. C_{OUT} must be a ceramic capacitor of at least 2.2μF, located close to the OUT pin. C_{OUT} also serves as the input decoupling capacitor for the charging circuit downstream of the protection IC.

REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

JANUARY 2016 – REV.A.1 to REV.A.2

Added Functional Block Diagram section 8

DECEMBER 2013 – REV.A to REV.A.1

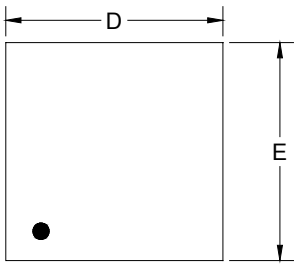
Added MSOP-8 (Exposed Pad) package ..... All

Changes from Original (OCTOBER 2012) to REV.A

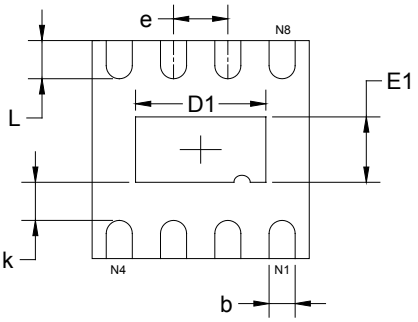
Changed from product preview to production data ..... All

PACKAGE OUTLINE DIMENSIONS

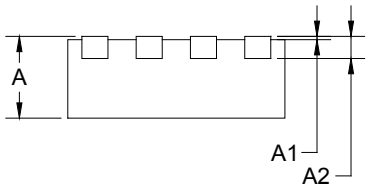
TDFN-2×2-8L



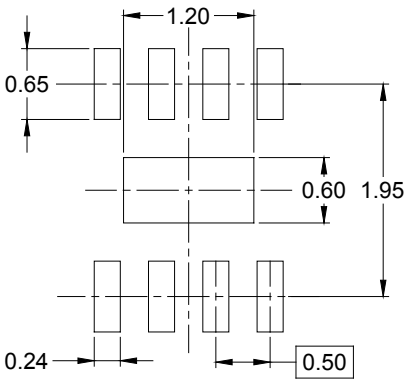
TOP VIEW



BOTTOM VIEW



SIDE VIEW

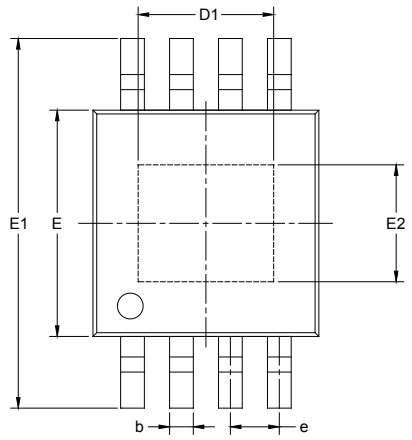


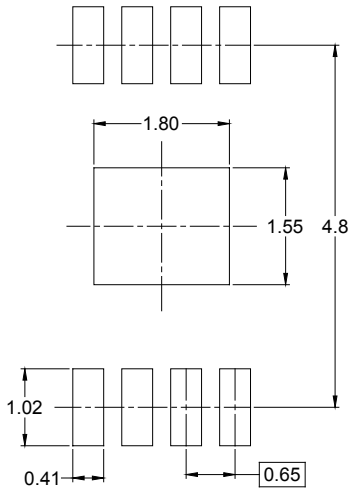
RECOMMENDED LAND PATTERN (Unit: mm)

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A2	0.203 REF		0.008 REF	
D	1.900	2.100	0.075	0.083
D1	1.100	1.300	0.043	0.051
E	1.900	2.100	0.075	0.083
E1	0.500	0.700	0.020	0.028
k	0.200 MIN		0.008 MIN	
b	0.180	0.300	0.007	0.012
e	0.500 TYP		0.020 TYP	
L	0.250	0.450	0.010	0.018

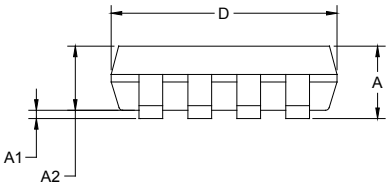
PACKAGE OUTLINE DIMENSIONS

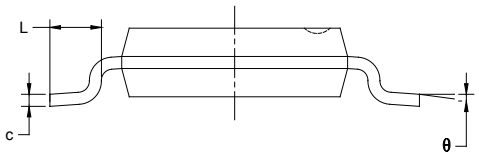
MSOP-8 (Exposed Pad)





RECOMMENDED LAND PATTERN (Unit: mm)

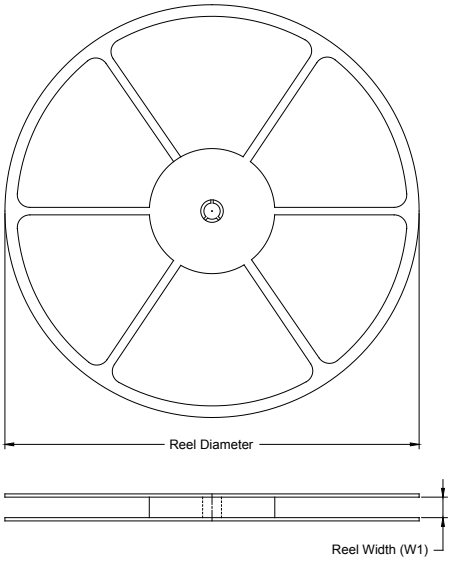




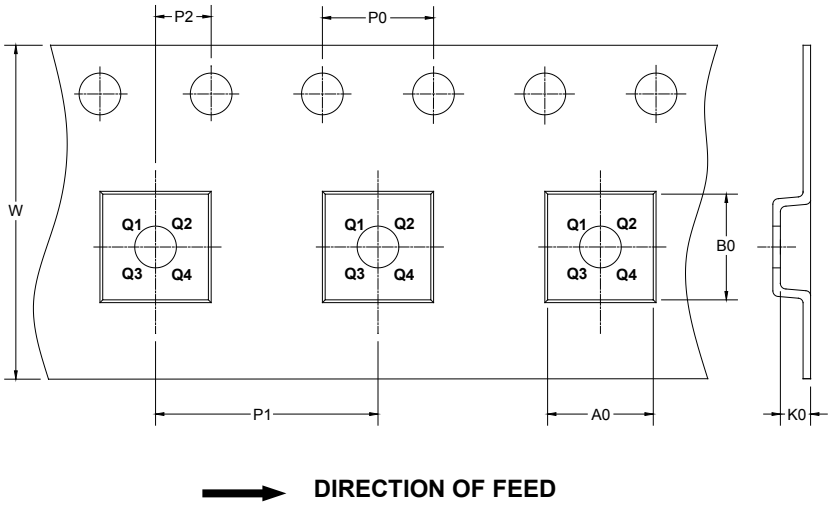
Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	0.820	1.100	0.032	0.043
A1	0.020	0.150	0.001	0.006
A2	0.750	0.950	0.030	0.037
b	0.250	0.380	0.010	0.015
c	0.090	0.230	0.004	0.009
D	2.900	3.100	0.114	0.122
D1	1.700	1.900	0.067	0.075
e	0.65 BSC		0.026 BSC	
E	2.900	3.100	0.114	0.122
E1	4.750	5.050	0.187	0.199
E2	1.450	1.650	0.057	0.065
L	0.400	0.800	0.016	0.031
θ	0°	6°	0°	6°

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



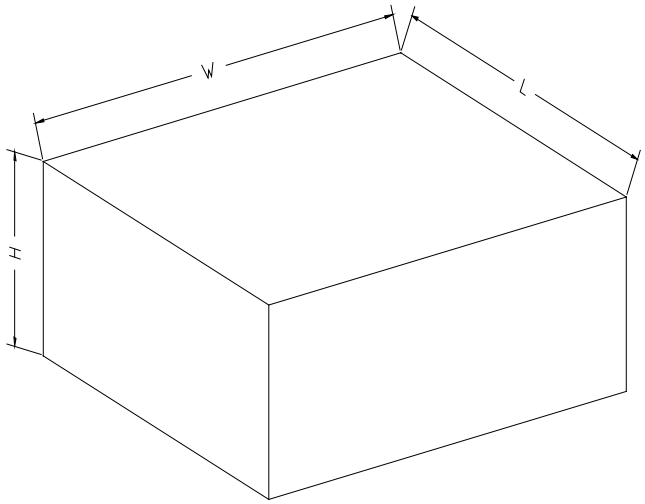
NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
TDFN-2×2-8L	7″	9.5	2.30	2.30	1.10	4.0	4.0	2.0	8.0	Q1
MSOP-8 (Exposed Pad)	13″	12.4	5.20	3.30	1.50	4.0	8.0	2.0	12.0	Q1

DD0001

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
7″ (Option)	368	227	224	8
7″	442	410	224	18
13″	386	280	370	5

DD0002