

[Document Title](#)

**256K x16 bit Super Low Power and Low Voltage Full CMOS Static RAM**

[Revision History](#)

<b>Revision No.</b>	<b>History</b>	<b>Date</b>	<b>Remark</b>
0.0	- . Initial Draft	May 26 2003	Preliminary
0.1	- . Add Pb-free part number	Feb. 13 2004	
0.2	- . I <sub>SB1</sub> (Max.) changed from 12uA to 6uA.	Mar. 31 2008	
0.3	- . Add 45ns part specification.	Apr. 2 2009	
	- . I <sub>SB1</sub> (Typ.) changed from 1uA to 0.25uA.		
	- . I <sub>SB1</sub> (Max.) changed from 6uA to 4uA.		
	- . Memory Function Guide updated in the last page.		
1.0	- . EM643FV16F(KGD), EM643FV16F series & EM643FV16FU series are unified to EM643FV16F Family.	Apr. 7 2009	Release

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The attached datasheets are provided by EMLSI reserve the right to change the specifications and products. EMLSI will answer to your questions about device. If you have any questions, please contact the EMLSI office.

**FEATURES**

- Process Technology : 0.18 $\mu$ m Full CMOS
- Organization : 256K x 16 bit
- Power Supply Voltage : 2.7V ~ 3.6V
- Low Data Retention Voltage : 1.5V(Min.)
- Three state output and TTL Compatible
- Package Type : VFBGA-48, 44-TSOP2

**GENERAL DESCRIPTION**

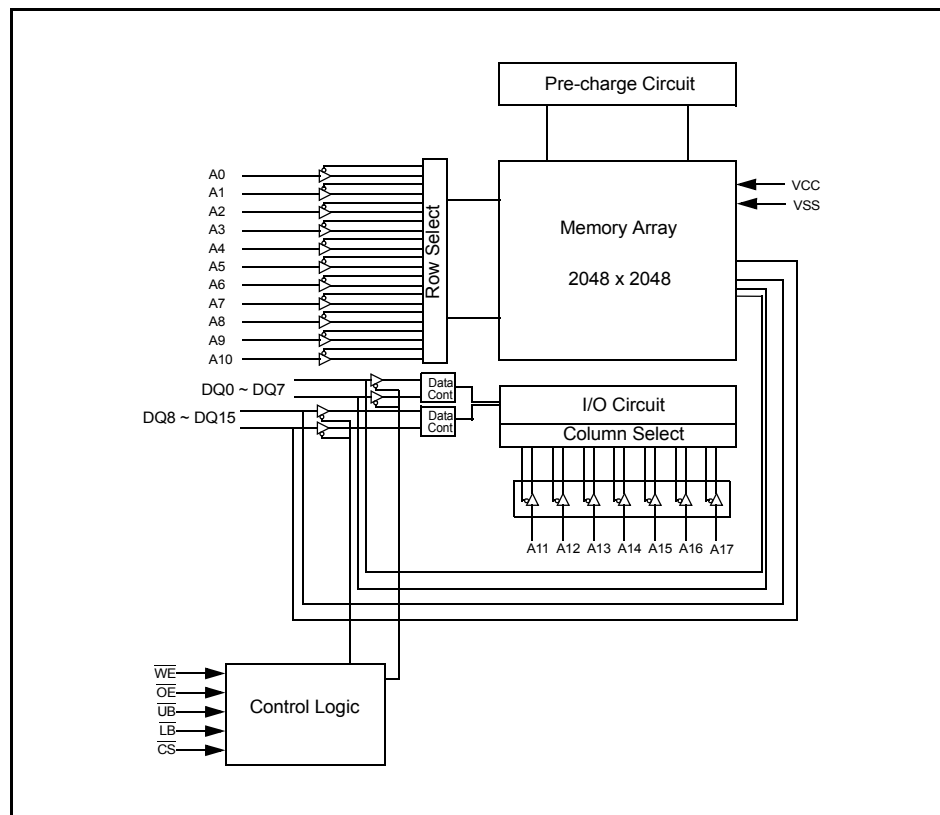
The EM643FV16F families are fabricated by EMLSI's advanced full CMOS process technology. The families support industrial temperature range and Chip Scale Package for user flexibility of system design. The families also supports low data retention voltage for battery back-up operation with low data retention current.

**PRODUCT FAMILY**

Product Family	Operating Temperature	Vcc Range	Speed	Power Dissipation		PKG Type
				Standby (I <sub>SB1</sub> , Typ.)	Operating (I <sub>CC1</sub> .Max.)	
EM643FV16F	Industrial (-40 ~ 85°C)	2.7 ~ 3.6 V	45/55/70 ns	0.25 $\mu$ A <sup>2</sup> )	3 mA	KGD
EM643FV16F - xx <sup>1</sup> )LF						VFBGA-48
EM643FV16FU - xx <sup>1</sup> )LF						44-TSOP2

1. "xx" represents speed.
2. Typical values are measured at Vcc=3.3V, T<sub>A</sub>=25°C and not 100% tested.

**FUNCTIONAL BLOCK DIAGRAM**

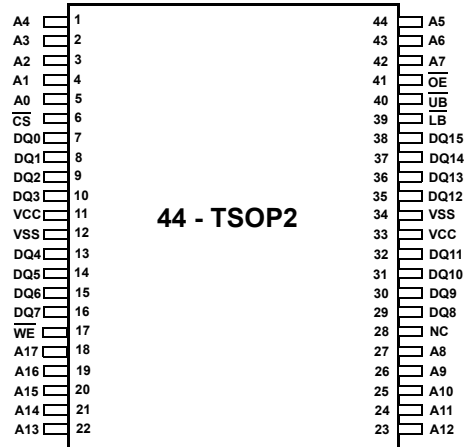


**PIN CONFIGURATIONS**

VFBGA-48 : Top view(ball down)

	1	2	3	4	5	6
A	$\overline{\text{LB}}$	$\overline{\text{OE}}$	A0	A1	A2	NC
B	DQ8	$\overline{\text{UB}}$	A3	A4	$\overline{\text{CS}}$	DQ0
C	DQ9	DQ10	A5	A6	DQ1	DQ2
D	VSS	DQ11	A17	A7	DQ3	VCC
E	VCC	DQ12	NC	A16	DQ4	VSS
F	DQ14	DQ13	A14	A15	DQ5	DQ6
G	DQ15	NC	A12	A13	$\overline{\text{WE}}$	DQ7
H	NC	A8	A9	A10	A11	NC

44 - TSOP2 : Top view



**PIN DESCRIPTION**

Name	Function	Name	Function
$\overline{\text{CS}}$	Chip Select input	VCC	Power Supply
$\overline{\text{OE}}$	Output Enable input	VSS	Ground
$\overline{\text{WE}}$	Write Enable input	$\overline{\text{UB}}$	Upper Byte (DQ8~DQ15)
A0~A17	Address inputs	$\overline{\text{LB}}$	Lower Byte (DQ0~DQ7)
DQ0~DQ15	Data inputs/outputs	NC	No Connection

**ABSOLUTE MAXIMUM RATINGS<sup>1)</sup>**

Parameter	Symbol	Ratings	Unit
Voltage on Any Pin Relative to Vss	$V_{IN}, V_{OUT}$	-0.2 to 4.0	V
Voltage on Vcc supply relative to Vss	$V_{CC}$	-0.2 to 4.0	V
Power Dissipation	$P_D$	1.0	W
Operating Temperature	$T_A$	-40 to 85	°C

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Functional operation should be restricted to recommended operating condition. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

**FUNCTIONAL DESCRIPTION**

$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	$\overline{LB}$	$\overline{UB}$	DQ0~7	DQ8~15	Mode	Power
H	X	X	X	X	High-Z	High-Z	Deselected	Stand by
X	X	X	H	H	High-Z	High-Z	Deselected	Stand by
L	H	H	L	X	High-Z	High-Z	Output Disabled	Active
L	H	H	X	L	High-Z	High-Z	Output Disabled	Active
L	L	H	L	H	Data Out	High-Z	Lower Byte Read	Active
L	L	H	H	L	High-Z	Data Out	Upper Byte Read	Active
L	L	H	L	L	Data Out	Data Out	Word Read	Active
L	X	L	L	H	Data In	High-Z	Lower Byte Write	Active
L	X	L	H	L	High-Z	Data In	Upper Byte Write	Active
L	X	L	L	L	Data In	Data In	Word Write	Active

**NOTE :** X means don't care. (Must be low or high state)

**RECOMMENDED DC OPERATING CONDITIONS** <sup>1)</sup>

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	$V_{CC}$	2.7	3.3	3.6	V
Ground	$V_{SS}$	0	0	0	V
Input high voltage	$V_{IH}$	2.2	-	$V_{CC} + 0.2^{2)}$	V
Input low voltage	$V_{IL}$	$-0.2^{3)}$	-	0.6	V

1.  $T_A = -40$  to  $85^\circ\text{C}$ , otherwise specified
2. Overshoot:  $V_{CC} + 2.0$  V in case of pulse width  $\leq 20\text{ns}$
3. Undershoot:  $-2.0$  V in case of pulse width  $\leq 20\text{ns}$
4. Overshoot and undershoot are sampled, not 100% tested.

**CAPACITANCE** <sup>1)</sup> ( $f = 1\text{MHz}$ ,  $T_A = 25^\circ\text{C}$ )

Item	Symbol	Test Condition	Min	Max	Unit
Input capacitance	$C_{IN}$	$V_{IN} = 0\text{V}$	-	8	pF
Input/Output capacitance	$C_{IO}$	$V_{IO} = 0\text{V}$	-	10	pF

1. Capacitance is sampled, not 100% tested.

**DC AND OPERATING CHARACTERISTICS**

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit			
Input leakage current	$I_{LI}$	$V_{IN} = V_{SS}$ to $V_{CC}$	-1	-	1	$\mu\text{A}$			
Output leakage current	$I_{LO}$	$\overline{CS} = V_{IH}$ or $\overline{OE} = V_{IH}$ or $\overline{WE} = V_{IL}$ or $\overline{LB} = \overline{UB} = V_{IH}$ $V_{IO} = V_{SS}$ to $V_{CC}$	-1	-	1	$\mu\text{A}$			
Operating power supply	$I_{CC}$	$I_{IO} = 0\text{mA}$ , $\overline{CS} = V_{IL}$ , $V_{IN} = V_{IH}$ or $V_{IL}$	-	-	3	mA			
Average operating current	$I_{CC1}$	Cycle time = $1\mu\text{s}$ , 100% duty, $I_{IO} = 0\text{mA}$ , $\overline{CS} \leq 0.2\text{V}$ , $\overline{LB} \leq 0.2\text{V}$ or/and $\overline{UB} \leq 0.2\text{V}$ , $V_{IN} \leq 0.2\text{V}$ or $V_{IN} \geq V_{CC} - 0.2\text{V}$	-	-	3	mA			
			$I_{CC2}$	Cycle time = Min, $I_{IO} = 0\text{mA}$ , 100% duty, $\overline{CS} = V_{IL}$ , $\overline{LB} = V_{IL}$ or/and $\overline{UB} = V_{IL}$ , $V_{IN} = V_{IL}$ or $V_{IH}$	45ns	-	-	35	mA
					55ns	-	-	30	
70ns	-	-	25						
Output low voltage	$V_{OL}$	$I_{OL} = 2.1\text{mA}$	-	-	0.4	V			
Output high voltage	$V_{OH}$	$I_{OH} = -1.0\text{mA}$	2.4	-	-	V			
Standby Current (TTL)	$I_{SB}$	$\overline{CS} = V_{IH}$ , Other inputs = $V_{IH}$ or $V_{IL}$	-	-	0.3	mA			
Standby Current (CMOS)	$I_{SB1}$	$\overline{CS} \geq V_{CC} - 0.2\text{V}$ , Other inputs = $0 \sim V_{CC}$ (Typ. condition : $V_{CC} = 3.3\text{V}$ @ $25^\circ\text{C}$ ) (Max. condition : $V_{CC} = 3.6\text{V}$ @ $85^\circ\text{C}$ )	LL LF	-	$0.25^{1)}$	4	$\mu\text{A}$		

1. Typical values are measured at  $V_{CC} = 3.3\text{V}$ ,  $T_A = 25^\circ\text{C}$  and not 100% tested.

### AC OPERATING CONDITIONS

#### Test Conditions (Test Load and Test Input/Output Reference)

Input Pulse Level : 0.4 to 2.2V

Input Rise and Fall Time : 5ns

Input and Output reference Voltage : 1.5V

Output Load (See right) :  $CL^1 = 100\text{pF} + 1 \text{ TTL}(70\text{ns})$

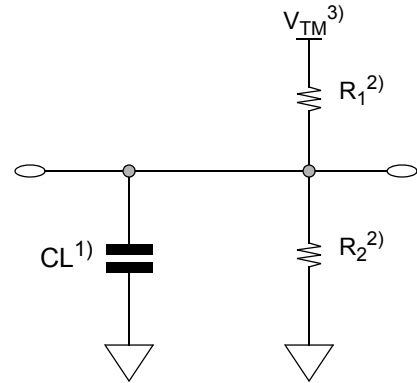
$CL^1 = 30\text{pF} + 1 \text{ TTL}(45\text{ns}/55\text{ns})$

1. Including scope and Jig capacitance

2.  $R_1=3070\Omega$ ,  $R_2=3150\Omega$

3.  $V_{TM}=2.8\text{V}$

4.  $CL = 5\text{pF} + 1 \text{ TTL}$  (measurement with tLZ, tOLZ, tHZ, tOHZ, tWHZ)



### READ CYCLE ( $V_{CC} = 2.7$ to $3.6\text{V}$ , $Gnd = 0\text{V}$ , $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$ )

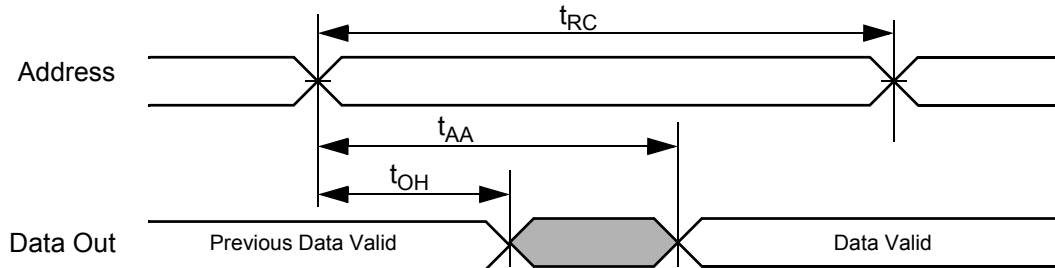
Parameter	Symbol	45ns		55ns		70ns		Unit
		Min	Max	Min	Max	Min	Max	
Read cycle time	$t_{RC}$	45	-	55	-	70	-	ns
Address access time	$t_{AA}$	-	45	-	55	-	70	ns
Chip select to output	$t_{CO}$	-	45	-	55	-	70	ns
Output enable to valid output	$t_{OE}$	-	20	-	25	-	35	ns
$\overline{UB}$ , $\overline{LB}$ access time	$t_{BA}$		20		25		35	ns
Chip select to low-Z output	$t_{LZ}$	10	-	10	-	10	-	ns
$\overline{UB}$ , $\overline{LB}$ enable to low-Z output	$t_{BLZ}$	5	-	5	-	5	-	ns
Output enable to low-Z output	$t_{OLZ}$	5	-	5	-	5	-	ns
Chip disable to high-Z output	$t_{HZ}$	0	20	0	20	0	25	ns
$\overline{UB}$ , $\overline{LB}$ disable to high-Z output	$t_{BHZ}$	0	20	0	20	0	25	ns
Output disable to high-Z output	$t_{OHZ}$	0	20	0	20	0	25	ns
Output hold from address change	$t_{OH}$	10	-	10	-	10	-	ns

### WRITE CYCLE ( $V_{CC} = 2.7$ to $3.6\text{V}$ , $Gnd = 0\text{V}$ , $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$ )

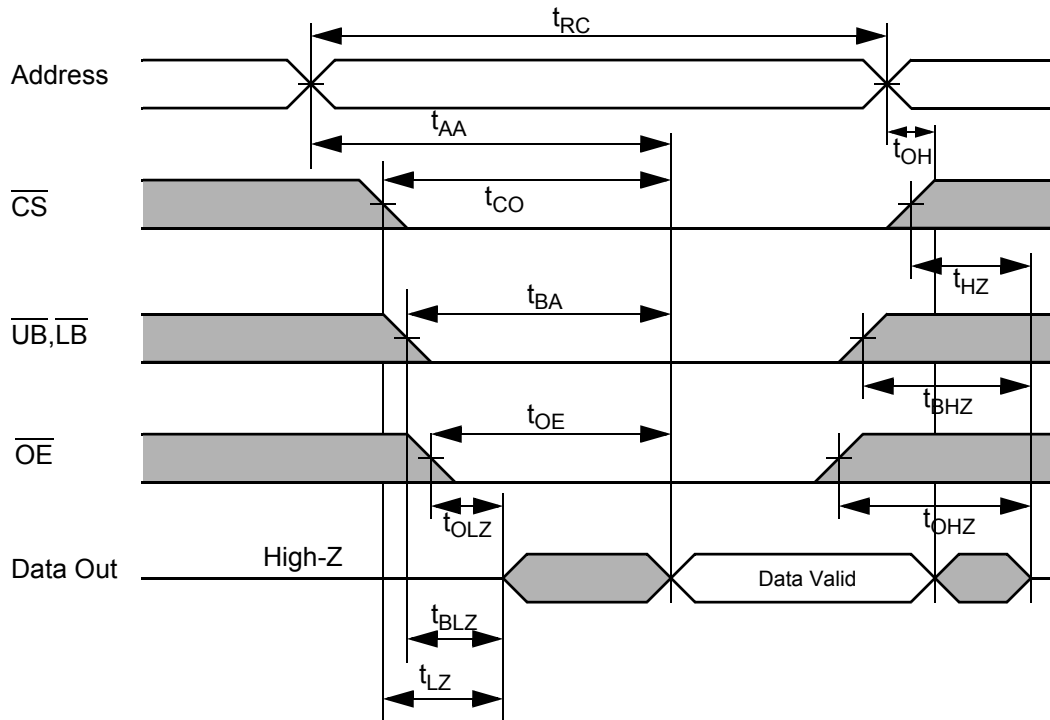
Parameter	Symbol	45ns		55ns		70ns		Unit
		Min	Max	Min	Max	Min	Max	
Write cycle time	$t_{WC}$	45	-	55	-	70	-	ns
Chip select to end of write	$t_{CW}$	35	-	45	-	60	-	ns
Address setup time	$t_{AS}$	0	-	0	-	0	-	ns
Address valid to end of write	$t_{AW}$	35	-	45	-	60	-	ns
$\overline{UB}$ , $\overline{LB}$ valid to end of write	$t_{BW}$	35	-	45	-	60	-	ns
Write pulse width	$t_{WP}$	35	-	40	-	55	-	ns
Write recovery time	$t_{WR}$	0	-	0	-	0	-	ns
Write to output high-Z	$t_{WHZ}$	0	20	0	20	0	25	ns
Data to write time overlap	$t_{DW}$	25		25		30		ns
Data hold from write time	$t_{DH}$	0	-	0	-	0	-	ns
End write to output low-Z	$t_{OW}$	5	-	5	-	5	-	ns

**TIMING DIAGRAMS**

**TIMING WAVEFORM OF READ CYCLE(1)** (Address Controlled,  $\overline{CS}=\overline{OE}=V_{IL}$ ,  $\overline{WE}=V_{IH}$ ,  $\overline{UB}$  or/and  $\overline{LB}=V_{IL}$ )



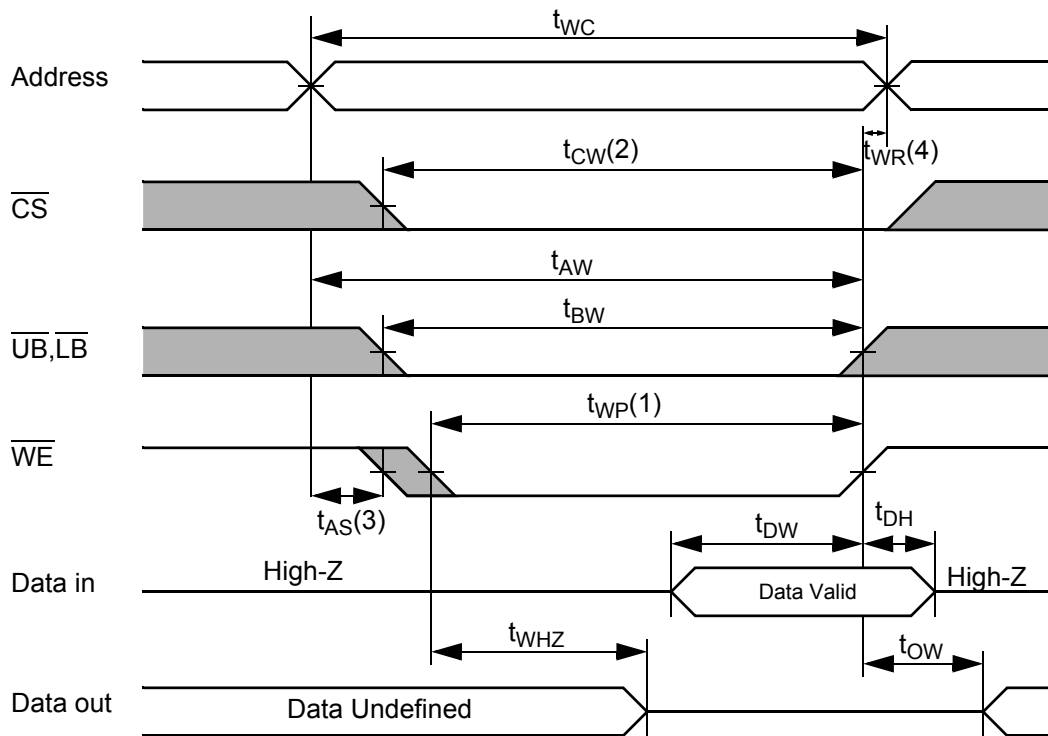
**TIMING WAVEFORM OF READ CYCLE(2)** ( $\overline{WE}=V_{IH}$ )



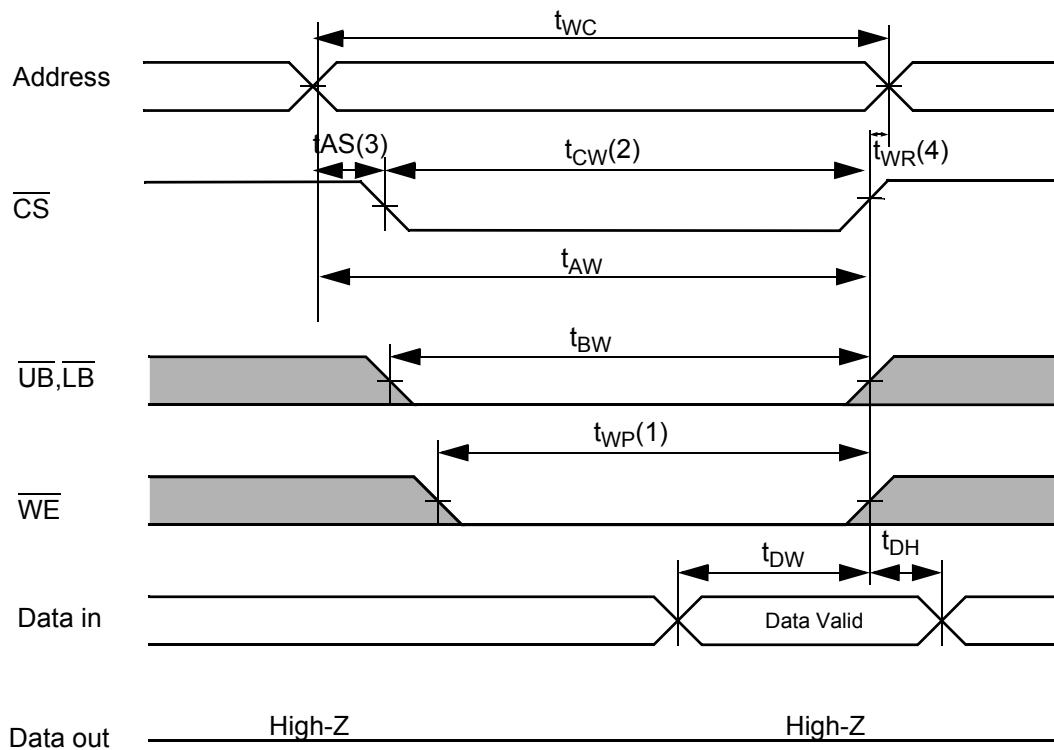
**NOTES (READ CYCLE)**

- $t_{HZ}$  and  $t_{OHZ}$  are defined as the outputs achieve the open circuit conditions and are not referenced to output voltage levels.
- At any given temperature and voltage condition,  $t_{HZ}(\text{Max.})$  is less than  $t_{LZ}(\text{Min.})$  both for a given device and from device to device interconnection.

**TIMING WAVEFORM OF WRITE CYCLE(1) ( $\overline{WE}$  Controlled)**

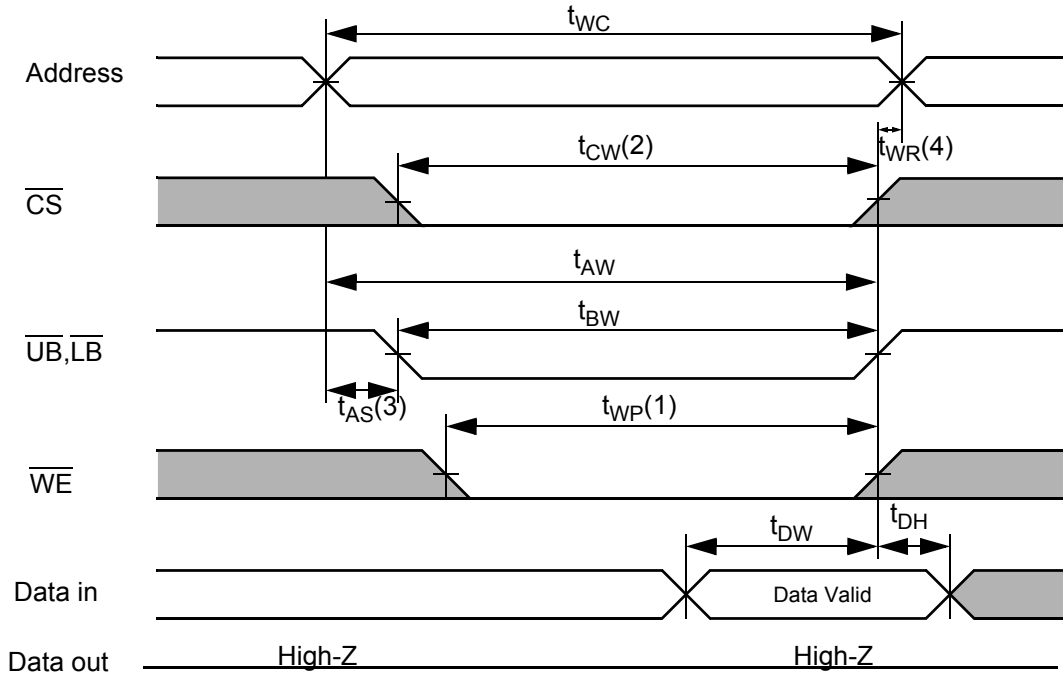


**TIMING WAVEFORM OF WRITE CYCLE(2) ( $\overline{CS}$  Controlled)**





**TIMING WAVEFORM OF WRITE CYCLE(3)** ( $\overline{UB}$ ,  $\overline{LB}$  Controlled)



**NOTES (WRITE CYCLE)**

1. A write occurs during the overlap( $t_{WP}$ ) of low  $\overline{CS}$  and low  $\overline{WE}$ . A write begins when  $\overline{CS}$  goes low and  $\overline{WE}$  goes low with asserting  $\overline{UB}$  or  $\overline{LB}$  for single byte operation or simultaneously asserting  $\overline{UB}$  and  $\overline{LB}$  for double byte operation. A write ends at the earliest transition when  $\overline{CS}$  goes high and  $\overline{WE}$  goes high. The  $t_{WP}$  is measured from the beginning of write to the end of write.
2.  $t_{CW}$  is measured from the  $\overline{CS}$  going low to end of write.
3.  $t_{AS}$  is measured from the address valid to the beginning of write.
4.  $t_{WR}$  is measured from the end of write to the address change.  $t_{WR}$  applied in case a write ends as  $\overline{CS}$  or  $\overline{WE}$  going high.

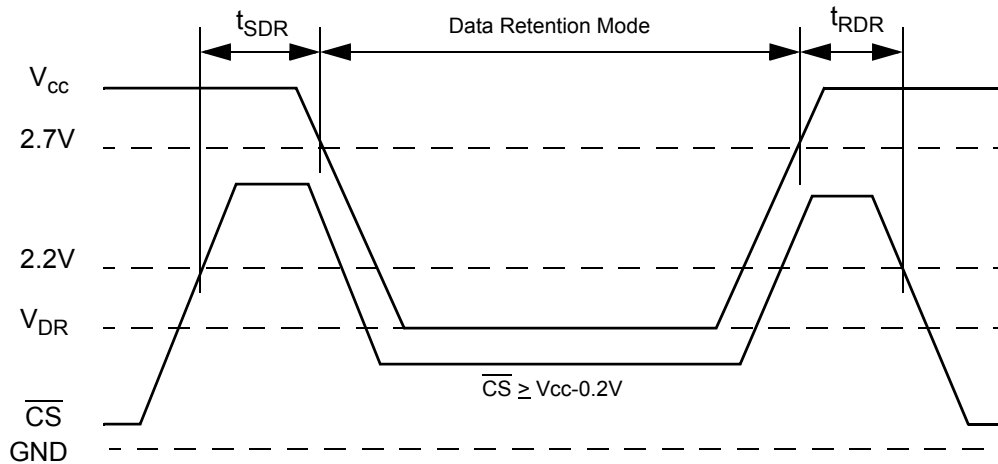
**DATA RETENTION CHARACTERISTICS**

Parameter	Symbol	Test Condition	Min	Typ <sup>2)</sup>	Max	Unit
V <sub>CC</sub> for Data Retention	V <sub>DR</sub>	I <sub>SB1</sub> Test Condition (Chip Disabled) <sup>1)</sup>	1.5	-	3.6	V
Data Retention Current	I <sub>DR</sub>	V <sub>CC</sub> =1.5V, I <sub>SB1</sub> Test Condition (Chip Disabled) <sup>1)</sup>	-	0.5	-	μA
Chip Deselect to Data Retention Time	t <sub>SDR</sub>	See data retention wave form	0	-	-	ns
Operation Recovery Time	t <sub>RDR</sub>		t <sub>RC</sub>	-	-	

**NOTES**

1. See the I<sub>SB1</sub> measurement condition of datasheet page 5.
2. Typical values are measured at T<sub>A</sub>=25°C and not 100% tested.

**DATA RETENTION WAVE FORM**

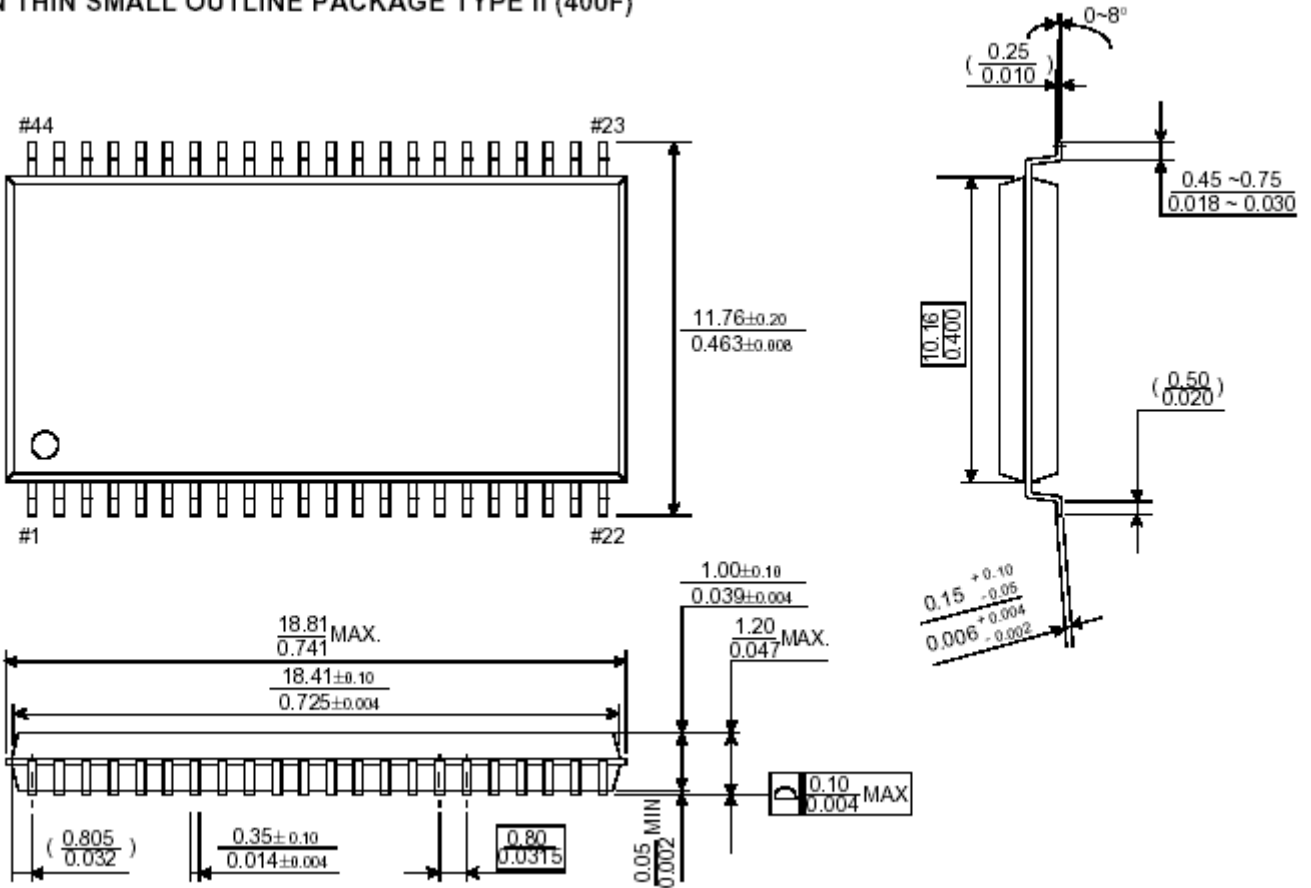


**PACKAGE DIMENSION**

44 - TSOP2 (0.8mm pin pitch)

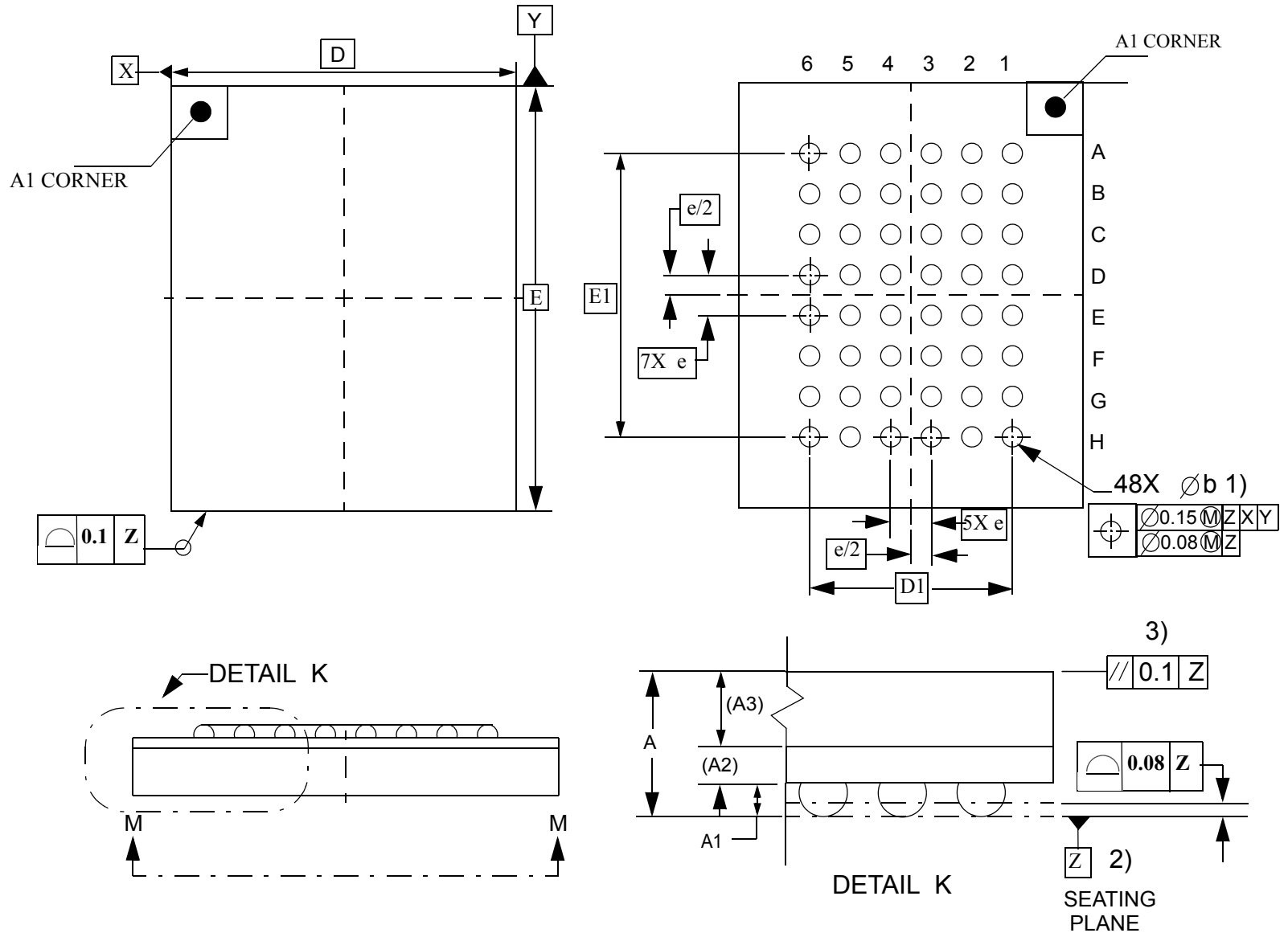
Unit : millimeters / inches

44 PIN THIN SMALL OUTLINE PACKAGE TYPE II (400F)



Unit: millimeters

VFBGA 48 BALLS (6X7X1 0.75mm ball pitch)



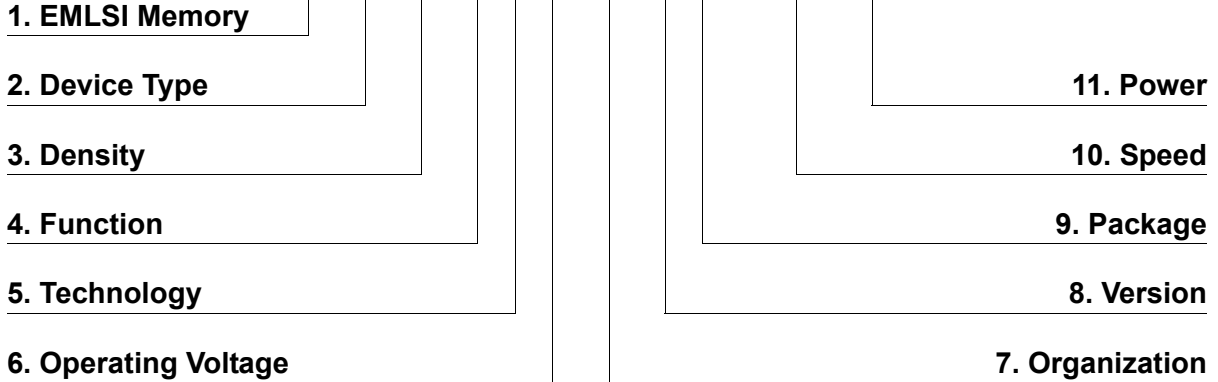
	Min.	NOR.	Max.
A	---		1
A1	0.22		0.32
A2		0.21 REF	
A3		0.45 REF	
b	0.32	5.25	0.42
D		6 BSC	
E		7 BSC	
e		0.75 BSC	
D1		0.35 BSC	
E1		5.25 BSC	

NOTES.

- 1). DIMENSION b IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO DATUM PLANE Z.
- 2). DATUM Z (SEATING PLANE) IS DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
- 3). PARALLELISM MEASUREMENT SHALL EXCLUDE ANY EFFECT OF MARK ON TOP SURFACE OF PACKAGE.

**MEMORY FUNCTION GUIDE**

EMXXXXXXXXXXXXX - XXXX



- 1. Memory Component
- 2. Device Type
  - 6 ----- Low Power SRAM
  - 7 ----- STRAM
  - C ----- CellularRAM
- 3. Density
  - 1 ----- 1M
  - 2 ----- 2M
  - 4 ----- 4M
  - 8 ----- 8M
  - 16 ----- 16M
  - 32 ----- 32M
  - 64 ----- 64M
  - 28 ----- 128M
- 4. Option
  - 0 ----- Dual CS (x8)
  - 1 ----- Single CS (x8)
  - 3 ----- Single CS / tBA=tOE (x16)
  - 4 ----- Single CS / tBA=tCO (x16)
  - 5 ----- Dual CS / tBA=tOE (x16)
  - 6 ----- Dual CS / tBA=tCO (x16)
- 5. Technology
  - F ----- Full CMOS
- 6. Operating Voltage
  - T ----- 5.0V
  - V ----- 3.3V
  - U ----- 3.0V
  - S ----- 2.5V
  - R ----- 2.0V
  - P ----- 1.8V
- 7. Organization
  - 8 ----- X8 bit
  - 16 ----- X16 bit
  - 32 ----- X32 bit

- 8. Version
  - Blank----- Mother die
  - A ----- 2 nd generation
  - B ----- 3 rd generation
  - C ----- 4 th generation
  - D ----- 5 th generation
  - E ----- 6 th generation
  - F ----- 7 th generation
  - G ----- 8 th generation
- 9. Package
  - Blank----- KGD, FBGA
  - S ----- 32 sTSOP1
  - T ----- 32 TSOP1
  - U ----- 44 TSOP2
  - V ----- 32 SOP
- 10. Speed
  - 45 ----- 45ns
  - 55 ----- 55ns
  - 60 ----- 60ns
  - 70 ----- 70ns
  - 85 ----- 85ns
  - 90 ----- 90ns
  - 10 ----- 100ns
  - 12 ----- 120ns
- 11. Power
  - LL ----- Low Low Power
  - LF ----- Low Low Power(Pb-free & Green)
  - L ----- Low Power
  - S ----- Standard Power