Specification for Approval

PRODUCT NAME: RGC16128064WR001
PRODUCT NO.: 9919407000

CUSTOMER
APPROVED BY
DATE:

RITDISPLAY CORP. APPROVED

REVISION RECORD

REV.	REVISION DESCRIPTION	REV. DATE	REMARK
X01	INITIAL RELEASE	2009. 09. 04	
X02	■ Add lifetime specifications ■ Add panel electrical specifications ■ Add notes of power on/off sequence ■ Add application circuit	2009. 09. 21	Page 6, 7, 8, 16 & 17
A01	■ Transfer from X version ■ Modify seal color (white→black) ■ Add the packing specification	2009. 12. 15	Page 19 & 20
A02	■ Modify product name (RGS16128064WR001→ RGC16128064WR001) ■ Add specification of luminance at -10℃. ■ Add specification of single tape position	2010. 03. 18	Page 1, 18 & 19
A03	■ Add appendix of precautions for using the OLED module	2014. 07. 22	Page 25~34

CONTENTS

1. SCOPE

This specification is to define the general provisions and quality requirements that apply to the supply of display cells manufactured by RiTdisplay. This document, together with the Module Ass'y Drawing, is the highest-level specification for this product.

2. WARRANTY

RiTdisplay warrants that the products delivered pursuant to this specification (or order) will conform to the agreed specifications for twelve (12) months from the shipping date ("Warranty Period"). RiTdisplay is obligated to repair or replace the products which are found to be defective or inconsistent with the specifications during the Warranty Period without charge, on condition that the products are stored or used as the conditions specified in the specifications. Nevertheless, RiTdisplay is not obligated to repair or replace the products without charge if the defects or inconsistency are caused by the force majeure or the reckless behaviors of the customer.
After the Warranty Period, all repairs or replacements of the products are subject to charge.

3. FEATURES

- Small molecular organic light emitting diode
- Color : White
- Panel matrix : 128*64
- Driver IC : SSD1325
- Excellent quick response time.
- Extremely thin thickness for best mechanism design : 1.61mm
- High contrast : 2000:1
- Wide viewing angle : 160°
- 8-bit 6800-series parallel interface, 8-bit 8080-series parallel interface, serial peripheral interface
- Wide range of operating temperature : -40 to 70 ℃
- Anti-glare polarizer.

4. MECHANICAL DATA

NO	ITEM	SPECIFICATION	UNIT
1	Dot Matrix	128 (W) x 64 (H)	dot
2	Dot Size	0.255 (W) x 0.255 (H)	mm^2
3	Dot Pitch	0.285 (W) x 0.285 (H)	mm^2
4	Aperture Rate	80	%
5	Active Area	36.45 (W) x 18.21 (H)	mm^2
6	Panel Size	41.9 (W) x 28 (H)	mm^2
7*	Panel Thickness	1.42 ± 0.1	mm
8	Module Size	41.9 (W) x 65.1 (H) x 1.61 (D)	mm^3
9	Diagonal A/A size	1.6	inch
10	Module Weight	3.75 ± 10%	gram

* Panel thickness includes substrate glass, cover glass and UV glue thickness.

5. MAXIMUM RATINGS

ITEM	MIN	MAX	UNIT	Condition	Remark
Supply Voltage (V_{DD})	-0.3	3.5	V	Ta = 25℃	IC maximum rating
Supply Voltage (Vcc)	8	16	V	Ta = 25℃	IC maximum rating
Operating Temp.	-40	70	℃		
Storage Temp	-40	85	℃		
Humidity	-	85	%		
Life Time	10,000	-	Hrs	100 cd/m^2, 50% checkerboard	Note (1)
Life Time	12,000	-	Hrs	80 cd/m^2, 50% checkerboard	Note (2)
Life Time	16,000	-	Hrs	60 cd/m^2, 50% checkerboard	Note (3)

Note:

(A) Under Vcc = 15V, Ta = 25℃, 50% RH.

(B) Life time is defined the amount of time when the luminance has decayed to less than 50% of the initial measured luminance.

(1) Setting of 100 cd/m^2 :

- Contrast setting : 0x45
- Frame rate : 105Hz
- Duty setting : 1/64

(2) Setting of 80 cd/m^2 :

- Contrast setting : 0x37
- Frame rate : 105Hz
- Duty setting : 1/64

(3) Setting of 60 cd/m^2 :

- Contrast setting : 0x29
- Frame rate : 105Hz
- Duty setting : 1/64

6. ELECTRICAL CHARACTERISTICS

6.1 D.C ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETERS	TEST CONDITION	MIN	TYP	MAX	UNIT
V_{CC}	Analog power supply (for OLED panel)	Ta=-20 °C to +70°C	14.5	15	15.5	V
V_{DD}	Digital power supply	Ta=-20 °C to +70°C	2.4	2.8	3.5	V
I_{DD}	Operating current for V_{DD} V_{DD} = 2.7V, V_{CC} = 12V, IREF = 10uA No panel attached, All Display ON	Contrast=7F	-	-	650	uA
I_{CC}	Operating current for V_{CC} V_{DD} = 2.7V, V_{CC} = 12V, IREF = 10uA No panel attached, All Display ON	Contrast=7F	-	700	-	uA
V_{IH}	Hi logic input level		0.8* V_{DD}	-	V_{DD}	V
V_{IL}	Low logic input level		0	-	0.2* V_{DD}	V
V_{OH}	Hi logic output level		0.9* V_{DD}	-	V_{DD}	V
V_{OL}	Low logic output level		0	-	0.1* V_{DD}	V
I_{SEG}	Segment on output current V_{DD}=2.7V, V_{CC}=12V, IREF=10uA, Display on, Segment pin under test is connected with a 20K resistive load to V_{SS}	Contrast=7F	270	300	370	uA
		Contrast=5F	-	225	-	uA
		Contrast=3F	-	150	-	uA
		Contrast=1F	-	75	-	uA

6.2 ELECTRO-OPTICAL CHARATERISTICS

PANEL ELECTRICAL SPECIFICATIONS

PARAMETER	MIN	TYP.	MAX	UNITS	COMMENTS
Normal mode current		25	27	mA	All pixels on (1)
Standby mode current		3	4	mA	Standby mode 10% pixels on (2)
Normal mode power consumption		375	405	mW	All pixels on (1)
Standby mode power consumption		45	60	mW	Standby mode 10% pixels on (2)
Normal Luminance	60	80		cd/m^2	Display Average
Standby Luminance		10		cd/m^2	Display Average
CIEx (White)	0.26	0.30	0.34		x, y (CIE 1931)
CIEy (White)	0.28	0.32	0.36		
Dark Room Contrast	2000:1				
Viewing Angle	160			degree	
Response Time		10		μs	

(1) Normal mode condition :

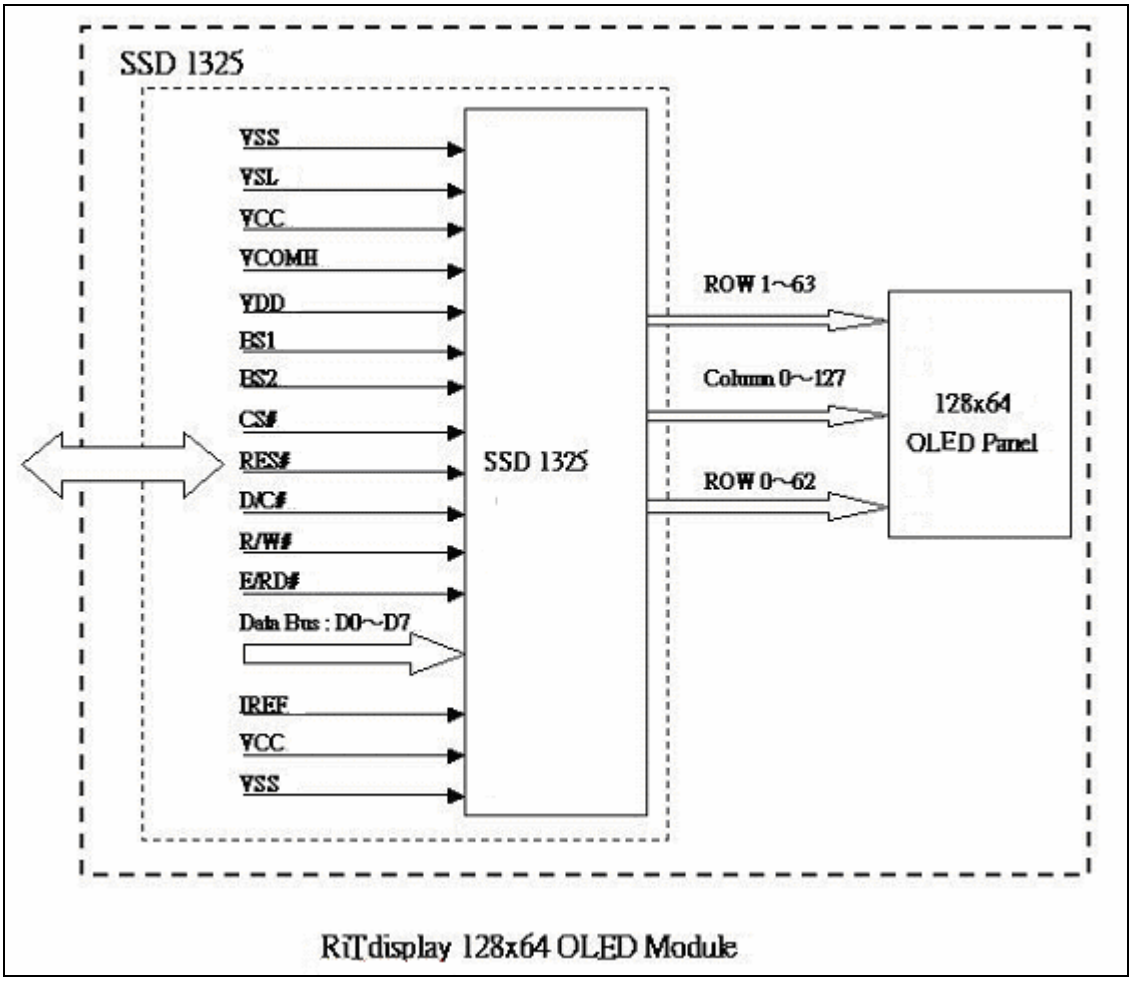
- Driving Voltage : 15V
- Contrast setting : 0x37
- Frame rate : 105Hz
- Duty setting : 1/64

(2) Standby mode condition :

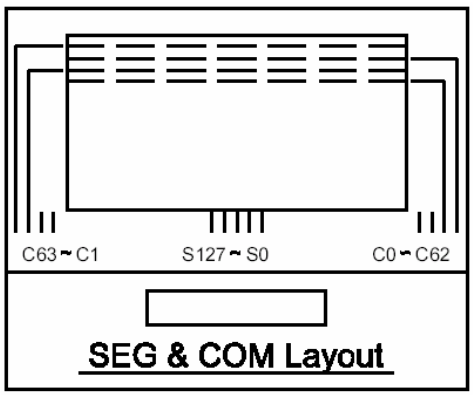
- Driving Voltage : 15V
- Contrast setting : 0x06
- Frame rate : 105Hz
- Duty setting : 1/64

7. INTERFACE

7.1 FUNCTION BLOCK DIAGRAM



7.2 PANEL LAYOUT DIAGRAM



7.3 PIN ASSIGNMENTS

Pin No.	Pin Name	Description
1	VSS	This is a ground pin.
2	VSL	This pin is the output pin for the voltage output low level for SEG signals. This pin can be kept NC or connected with a capacitor to VSS for stability.
3	VCC	Positive OLED high voltage power supply
4	VCOMH	The COM voltage reference pin, this pin should be connected to ground through a capacitor.
5	VDD	Voltage power supply for logic
6	BS1	Interface select pin
7	BS2	Interface select pin
8	CS#	Chip select pin. The driver IC will be selected When CS pin is active low.
9	RES#	Hardware reset signal
10	D/C#	Data/Command control pin. When it pulled high, the input at D0-D7 is treated as display data. When it pulled low, the input at D0-D7 is transferred to command register
11	R/W#	Write strobe signal and reads data at the low level
12	E(RD#)	Read strobe signal and reads data at the low level
13	D0	8-bit data bus
14	D1	8-bit data bus
15	D2	8-bit data bus
16	D3	8-bit data bus
17	D4	8-bit data bus
18	D5	8-bit data bus
19	D6	8-bit data bus
20	D7	8-bit data bus
21	IREF	The current reference input pin, this pin should be connected to ground through a resistor.
22	VCC	Positive OLED high voltage power supply
23	NC	No connection.
24	VSS	This is a ground pin.

7.4 GRAPHIC DISPLAY DATA RAM ADDRESS MAP

The GDDRAM is a bit mapped static RAM holding the bit pattern to be displayed. The size of the RAM is 128x80x4 bits. For mechanical flexibility, re-mapping on both Segment and Common outputs can be selected by software. (Refer to Table 3-7 for GDDRAM address map description)

		SEG0	SEG1	SEG2	SEG3		SEG124	SEG125	SEG126	SEG127	SEG Outputs
		00		01			3E		3F		Column Address
COM0	00	D0[3:0]	D0[7:4]	D1[3:0]	D1[7:4]		D62[3:0]	D62[7:4]	D63[3:0]	D63[7:4]	(HEX)
COM1	01	D64[3:0]	D64[7:4]	D65[3:0]	D65[7:4]		D126[3:0]	D126[7:4]	D127[3:0]	D127[7:4]	
|	|									
COM78	4E	D4992[3:0]	D4992[7:4]	D4993[3:0]	D4993[7:4]		D5054[3:0]	D5054[7:4]	D5055[3:0]	D5055[7:4]	
COM79	4F	D5056[3:0]	D5056[7:4]	D5057[3:0]	D5057[7:4]		D5118[3:0]	D5118[7:4]	D5119[3:0]	D5119[7:4]	
COM Outputs	Row Address (HEX)										

(Display Startline=0)

Table 3– GDDRAM address map showing Horizontal Address Increment A[2]=0, Column Address Re-map A[0]=0, Nibble Re-map A[1]=0, COM Re-map A[4]=0, and Display Start Line=00H (Data byte sequence: D0, D1, … , D5118, D5119)

		SEG0	SEG1	SEG2	SEG3		SEG124	SEG125	SEG126	SEG127	SEG Outputs
		00		01			3E		3F		Column Address
COM0	00	D0[3:0]	D0[7:4]	D80[3:0]	D80[7:4]		D4960[3:0]	D4960[7:4]	D5040[3:0]	D5040[7:4]	(HEX)
COM1	01	D1[3:0]	D1[7:4]	D81[3:0]	D81[7:4]		D4961[3:0]	D4961[7:4]	D5041[3:0]	D5041[7:4]	
|	|									
COM78	4E	D78[3:0]	D78[7:4]	D158[3:0]	D158[7:4]		D5038[3:0]	D5038[7:4]	D5118[3:0]	D5118[7:4]	
COM79	4F	D79[3:0]	D79[7:4]	D159[3:0]	D159[7:4]		D5039[3:0]	D5039[7:4]	D5119[3:0]	D5119[7:4]	
COM Outputs	Row Address (HEX)										

(Display Startline=0)

Table 4–GDDRAM address map showing Vertical Address Increment A[2]=1, Column Address Re-map A[0]=0, Nibble Re-map A[1]=0, COM Re-map A[4]=0, and Display Start Line=00H (Data byte sequence: D0, D1, … , D5118, D5119)

		SEG0	SEG1	SEG2	SEG3		SEG124	SEG125	SEG126	SEG127
		3F		3E			01		00	
COM0	00	D63[7:4]	D63[3:0]	D62[7:4]	D62[3:0]		D1[7:4]	D1[3:0]	D0[7:4]	D0[3:0]
COM1	01	D127[7:4]	D127[3:0]	D126[7:4]	D126[3:0]		D65[7:4]	D65[3:0]	D64[7:4]	D64[3:0]
|	|								
COM78	4E	D5055[7:4]	D5055[3:0]	D5054[7:4]	D5054[3:0]		D4993[7:4]	D4993[3:0]	D4992[7:4]	D4992[3:0]
COM79	4F	D5119[7:4]	D5119[3:0]	D5118[7:4]	D5118[3:0]		D5057[7:4]	D5057[3:0]	D5056[7:4]	D5056[3:0]

SEG Outputs Column Address (HEX)

COM Outputs | Row Address (HEX)

(Display Startline=0)

Table 5–GDDRAM address map showing Horizontal Address Increment A[2]=0, Column Address Re-map A[0]=1, Nibble Re-map A[1]=1, COM Re-map A[4]=0, and Display Start Line=00H (Data byte sequence: D0, D1, … , D5118, D5119)

		SEG0	SEG1	SEG2	SEG3		SEG124	SEG125	SEG126	SEG127
		00		01			3E		3F	
COM15	0F	D0[3:0]	D0[7:4]	D1[3:0]	D1[7:4]		D62[3:0]	D62[7:4]	D63[3:0]	D63[7:4]
COM14	0E	D64[3:0]	D64[7:4]	D65[3:0]	D65[7:4]		D126[3:0]	D126[7:4]	D127[3:0]	D127[7:4]
|	|								
COM17	11	D4992[3:0]	D4992[7:4]	D4993[3:0]	D4993[7:4]		D5054[3:0]	D5054[7:4]	D5055[3:0]	D5055[7:4]
COM16	10	D5056[3:0]	D5056[7:4]	D5057[3:0]	D5057[7:4]		D5118[3:0]	D5118[7:4]	D5119[3:0]	D5119[7:4]

SEG Outputs Column Address (HEX)

COM Outputs | Row Address (HEX)

(Display Startline=10H)

Table 6–GDDRAM address map showing Horizontal Address Increment A[2]=0, Column Address Re-map A[0]=0, Nibble Re-map A[1]=0, COM Re-map A[4]=1, and Display Start Line=16H (Data byte sequence: D0, D1, … , D5118, D5119)

		SEG0	SEG1	SEG2	SEG3		SEG124	SEG125	SEG126	SEG127
		00		01			3E		3F	
COM0	00									
COM1	01			D0[3:0]	D0[7:4]		D61[3:0]	D61[7:4]		
|	|								
COM78	4E			D4774[3:0]	D4774[7:4]		D4835[3:0]	D4835[7:4]		
COM79	4F									

SEG Outputs Column Address (HEX)

COM Outputs | Row Address (HEX)

(Display Startline=0)

Table 7–GDDRAM address map showing Horizontal Address Increment A[2]=0, Column Address Re-map A[0]=0, Nibble Re-map A[1]=0, COM Re-map A[4]=0, Display Start Line=00H (Data byte sequence: D0, D1, … , D4834, D4835), Column Start Address=01H, Column End Address=3EH, Row Start Address=01H and Row End Address=4EH

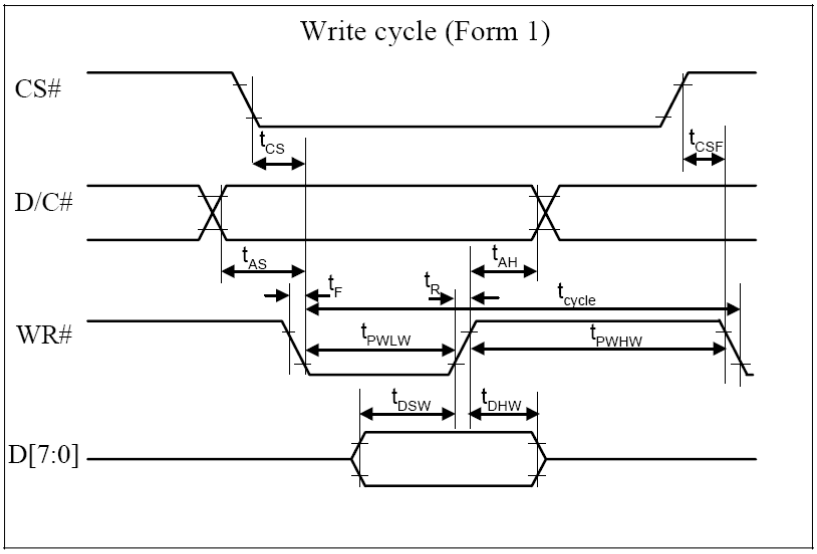
7.5 INTERFACE TIMING CHART

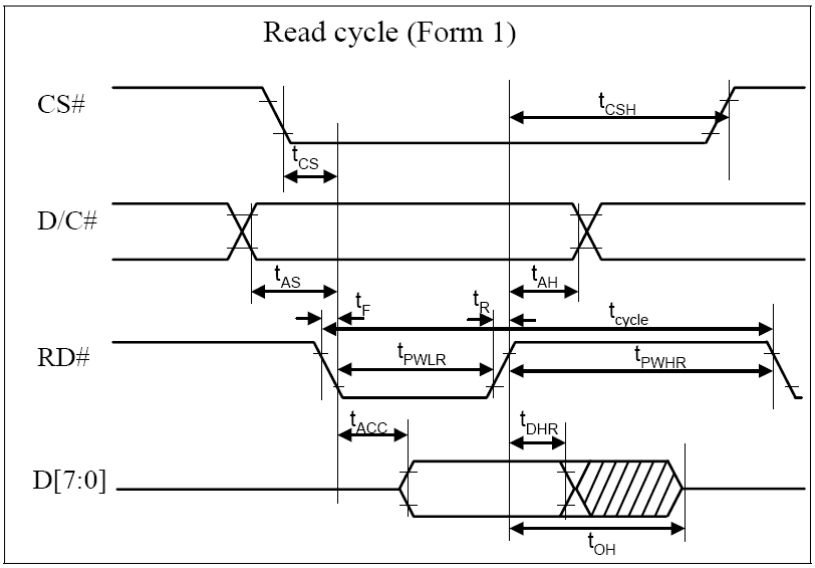
8080-Series MPU Parallel Interface Timing Characteristics

(V_{DD} - V_{SS} = 2.4 to 3.5V, T_A = 25°C)

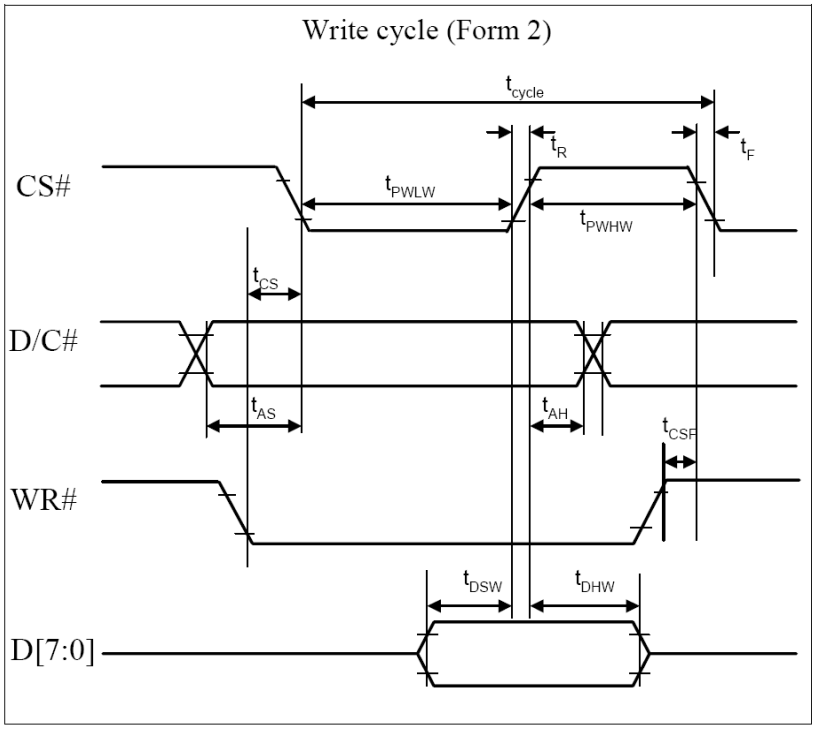
Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	300	-	-	ns
t_{AS}	Address Setup Time	10	-	-	ns
t_{AH}	Address Hold Time	0	-	-	ns
t_{DSW}	Write Data Setup Time	40	-	-	ns
t_{DHW}	Write Data Hold Time	15	-	-	ns
t_{DHR}	Read Data Hold Time	20	-	-	ns
t_{OH}	Output Disable Time	-	-	70	ns
t_{ACC}	Access Time	-	-	140	ns
t_{PWLR}	Read Low Time	120	-	-	ns
t_{PWLW}	Write Low Time	60	-	-	ns
t_{PWHR}	Read High Time	60	-	-	ns
t_{PWHW}	Write High Time	60	-	-	ns
t_R	Rise Time	-	-	15	ns
t_F	Fall Time	-	-	15	ns
t_{CS}	Chip select setup time	0	-	-	ns
t_{CSH}	Chip select hold time to read signal	0	-	-	ns
t_{CSF}	Chip select hold time	20	-	-	ns

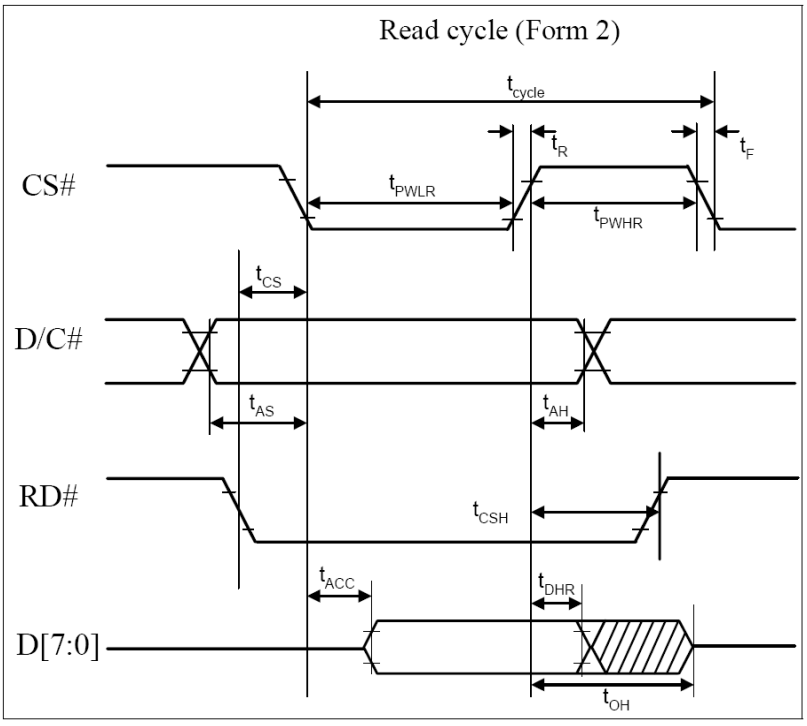
8080-series parallel interface characteristics (Form 1)





8080-series parallel interface characteristics (Form2)



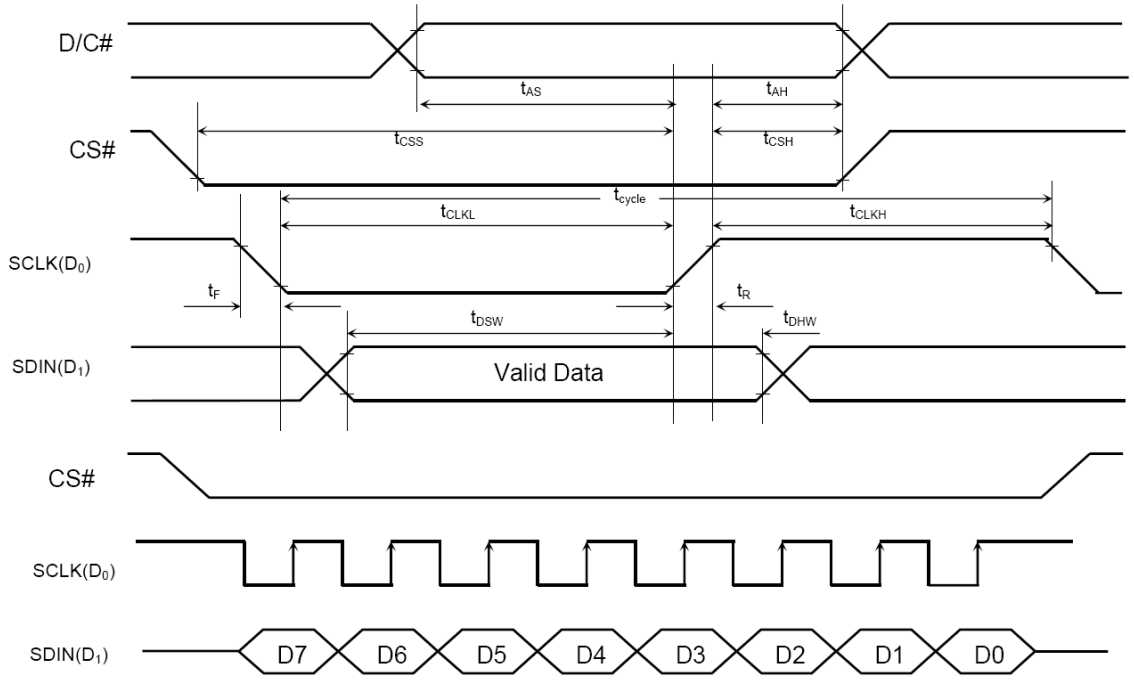


Serial Interface Timing Characteristics

(V_{DD} - V_{SS} = 2.4 to 3.5V, T_A = 25°C)

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	250	-	-	ns
t_{AS}	Address Setup Time	150	-	-	ns
t_{AH}	Address Hold Time	150	-	-	ns
t_{CSS}	Chip Select Setup Time	120	-	-	ns
t_{CSH}	Chip Select Hold Time	60	-	-	ns
t_{DSW}	Write Data Setup Time	100	-	-	ns
t_{DHW}	Write Data Hold Time	100	-	-	ns
t_{CLKL}	Clock Low Time	100	-	-	ns
t_{CLKH}	Clock High Time	100	-	-	ns
t_R	Rise Time	-	-	15	ns
t_F	Fall Time	-	-	15	ns

Serial Interface Characteristics

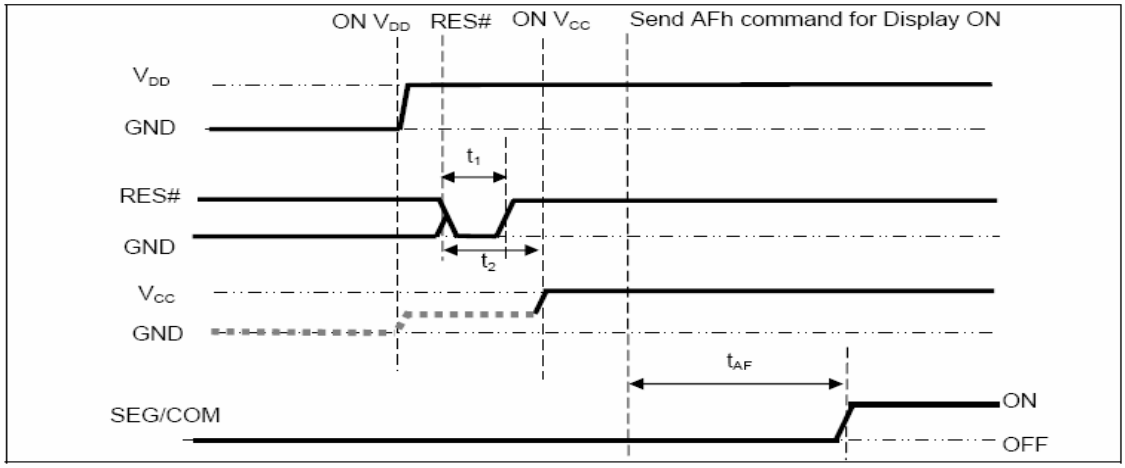


8. POWER ON / OFF SEQUENCE & APPLICATION CIRCUIT

8.1 POWER ON / OFF SEQUENCE

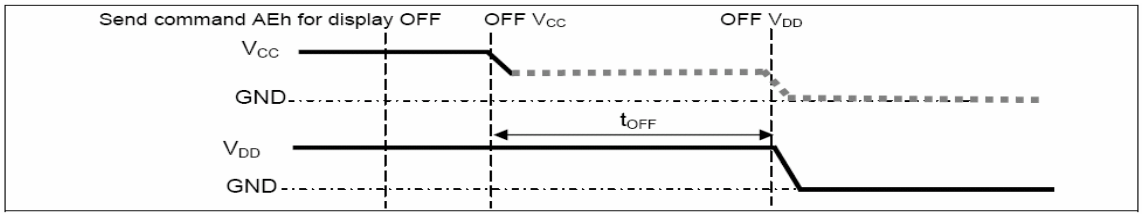
Power ON sequence:

1. Power ON V_{DD}.
2. After V_{DD} become stable, set RES# pin LOW (logic low) for at least 3us(t_1) and then HIGH (logic high).
3. After set RES# pin LOW (logic low), wait for at least 3us(t_2).Then Power ON V_{CC}.(1)
4. After V_{CC} become stable, send command AFh for display ON. SEG/COM will be ON after 100ms(t_{AF}).



Power OFF sequence:

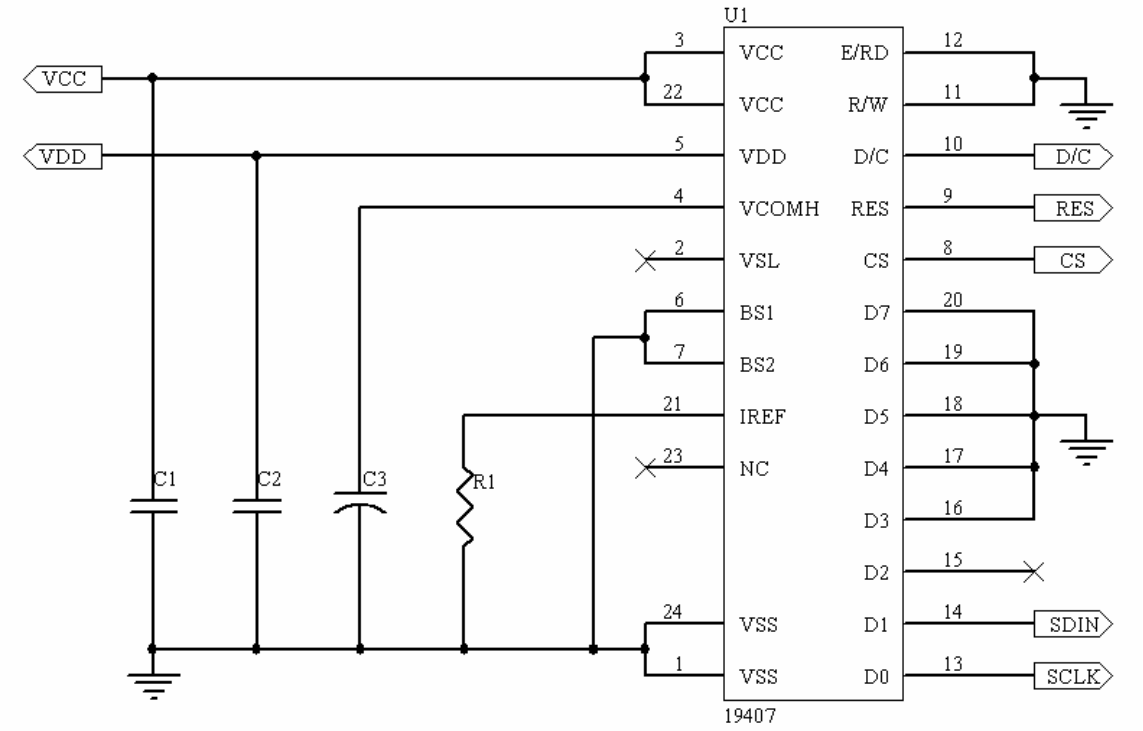
1. Send command AEh for display OFF.
2. Wait until panel discharges completely.
3. Power OFF V_{CC}. (1), (2)
4. Wait for t_{OFF}. Power OFF V_{DD}. (where Minimum t_{OFF}=80ms, Typical t_{OFF}=100ms)



Note:

(1) Since an ESD protection circuit is connected between VDD and VCC, VCC becomes lower than VDD whenever VDD is ON and VCC is OFF as shown in the dotted line of VCC in above figures.
(2) VCC should be kept float (disable) when it is OFF.
(3) Power Pins (VDD, VCC) can never be pulled to ground under any circumstance.
(4) The register values are reset after t1.
(5) VDD should not be Power OFF before VCC Power OFF.

8.2 APPLICATION CIRCUIT



Recommend components:

C1: 2.2uF/25V (0805)

C2: 1uF/16V (0603)

C3: 4.7uF/35V (Tantalum type), or VISHAY (572D475X0025A2T)

R1: 1M ohm/1% (0603)

Notes: This circuit is for SPI interface.

8.3 COMMAND TABLE

Refer to SSD1325 IC Spec.

9. RELIABILITY TEST CONDITIONS

No.	Items	Specification	Quantity
1	High temp. (Non-operation)	85℃, 240hrs	5
2	High temp. (Operation)	70℃, 120hrs	5
3	Low temp. (Operation)	-40℃, 120hrs	5
4	High temp. / High humidity (Operation)	65℃, 90%RH, 120hrs	5
5	Thermal shock (Non-operation)	-40℃ ~85℃ (-40℃ /30min; transit /3min; 85℃ /30min; transit /3min) 1cycle: 66min, 100 cycles	5
6	Vibration	Frequency : 5~50HZ, 0.5G Scan rate : 1 oct/min Time : 2 hrs/axis Test axis : X, Y, Z	1 Carton
7	Drop	Height: 120cm Sequence : 1 angle、3 edges and 6 faces Cycles: 1	1 Carton
8	ESD (Non-operation)	Air discharge model, ±8kV, 10 times	5

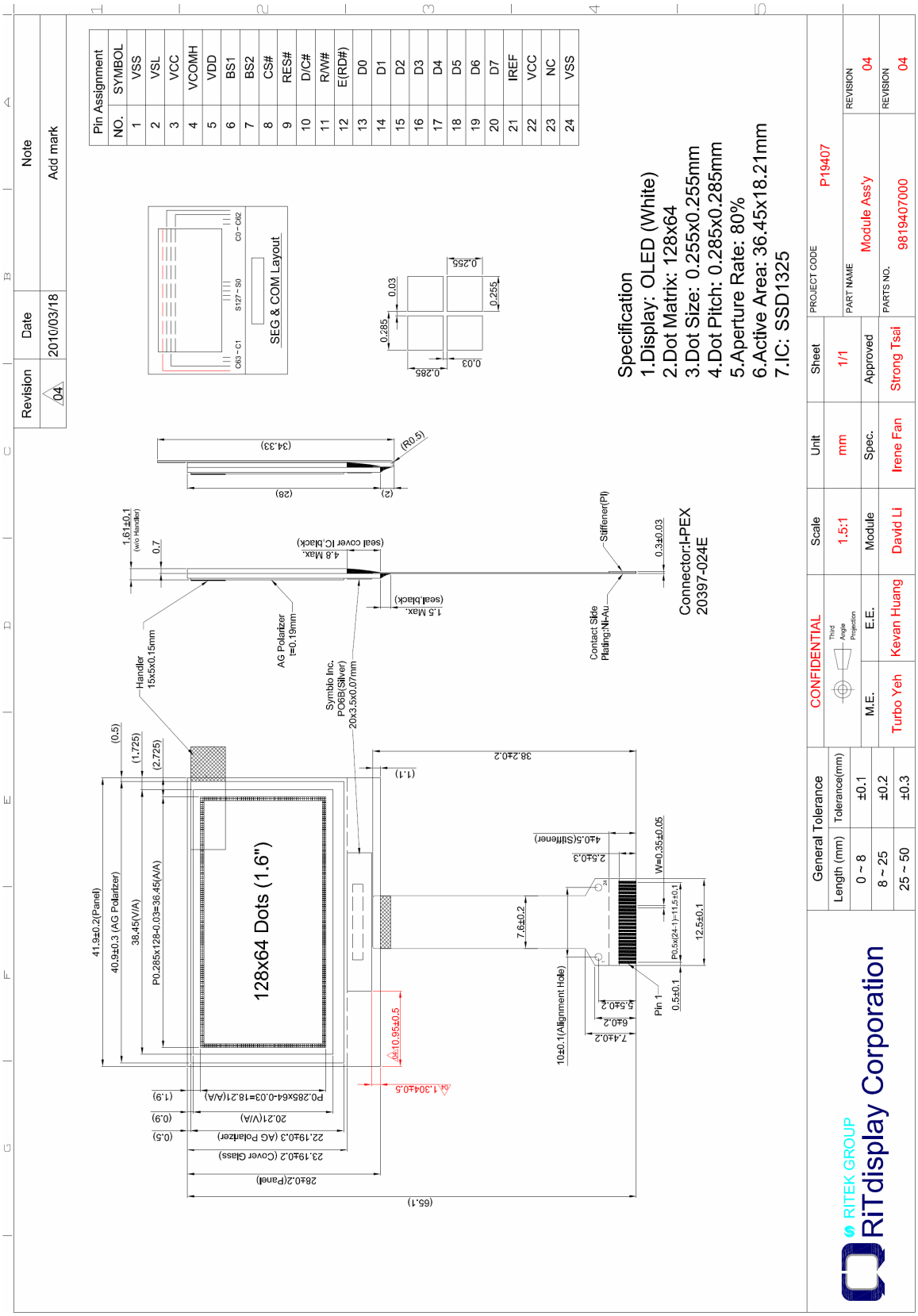
Test and measurement conditions

1. All measurements shall not be started until the specimens attain to temperature stability.
2. All-pixels-on is used as operation test pattern.
3. The degradation of Polarizer are ignored for item 1, 4 & 5.
4. The brightness decay will be less than 40% if operating at -10℃.

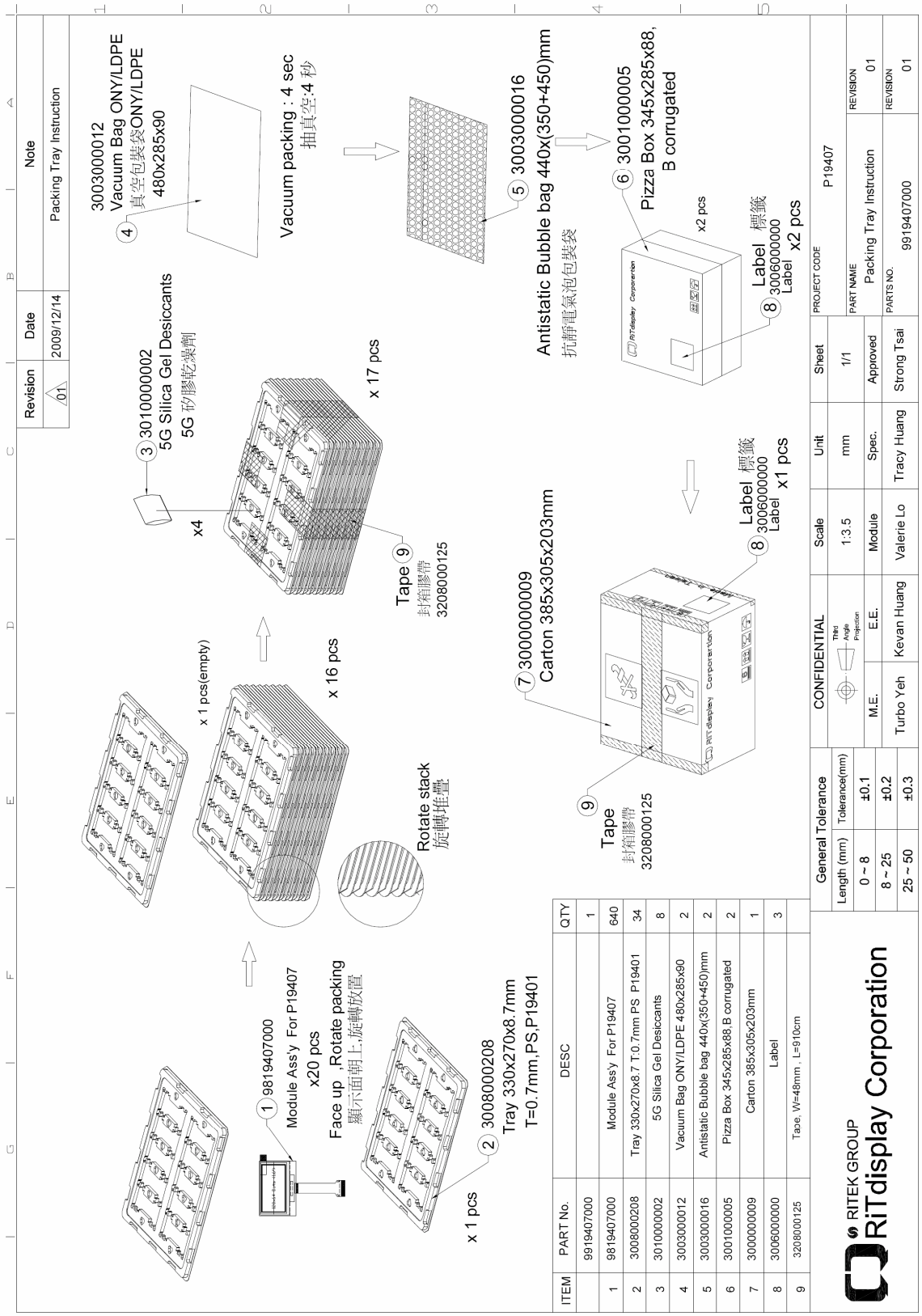
Evaluation criteria

1. The function test is OK.
2. No observable defects.
3. Luminance: > 50% of initial value.
4. Current consumption: within ± 50% of initial value.

10. EXTERNAL DIMENSION



11. PACKING SPECIFICATION



12. APPENDIXES

APPENDIX 1: DEFINITIONS

A. DEFINITION OF CHROMATICITY COORDINATE

The chromaticity coordinate is defined as the coordinate value on the CIE 1931 color chart for R, G, B, W.

B. DEFINITION OF CONTRAST RATIO

The contrast ratio is defined as the following formula:

$$\text{Contrast Ratio} = \frac{\text{Luminance of all pixels on measurement}}{\text{Luminance of all pixels off measurement}}$$

C. DEFINITION OF RESPONSE TIME

The definition of turn-on response time Tr is the time interval between a pixel reaching 10% of steady state luminance and 90% of steady state luminance. The definition of turn-off response time Tf is the time interval between a pixel reaching 90% of steady state luminance and 10% of steady state luminance. It is shown in Figure 2.

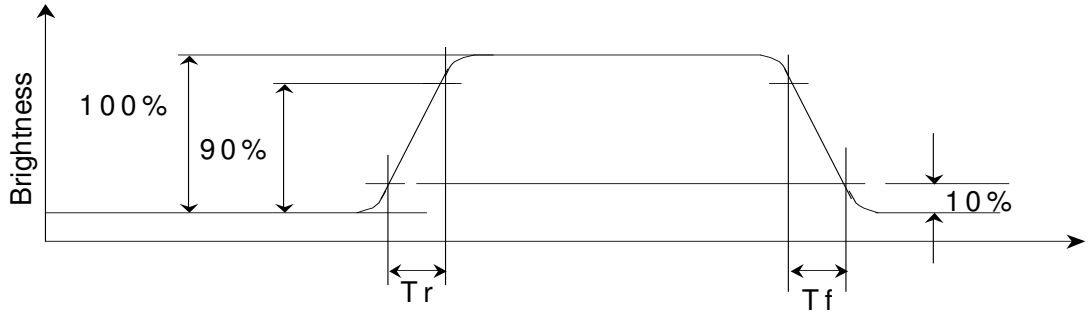


Figure 2: Response time

D. DEFINITION OF VIEWING ANGLE

The viewing angle is defined as Figure 3. Horizontal and vertical (H & V) angles are determined for viewing directions where luminance varies by 50% of the perpendicular value.

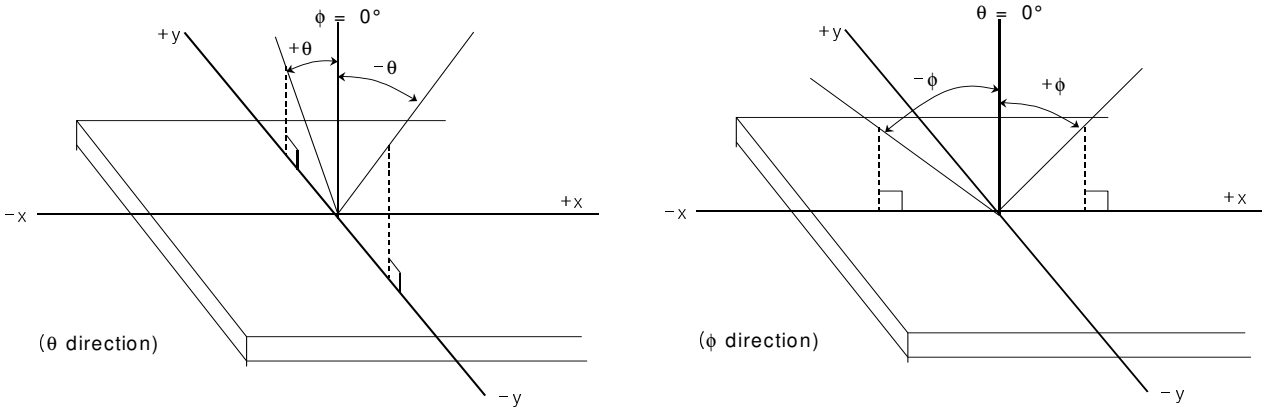
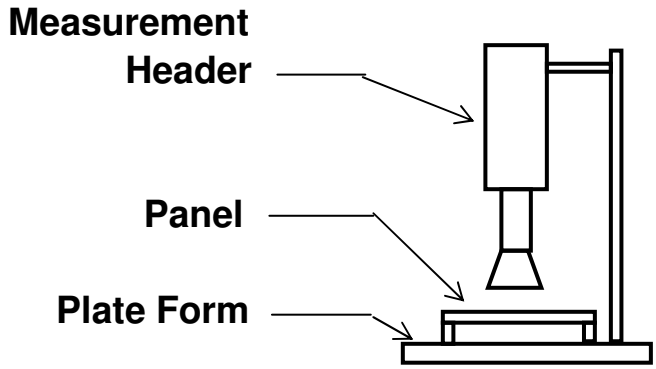


Figure 3: Viewing Angle

APPENDIX 2: MEASUREMENT APPARATUS

A. LUMINANCE/COLOR COORDINATE

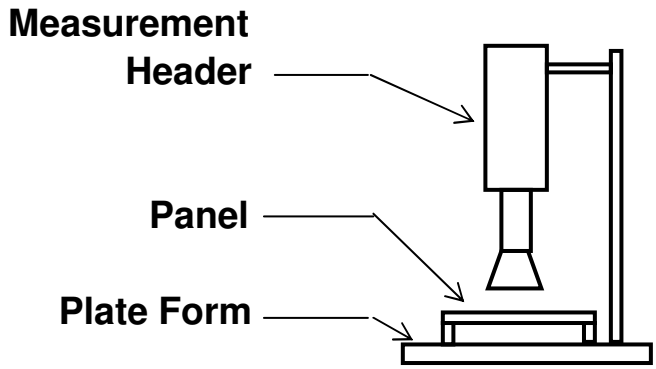
PHOTO RESEARCH PR-705, MINOLTA CS-100



**PR-705 /
MINOLTA CS-100
Color Analyzer**

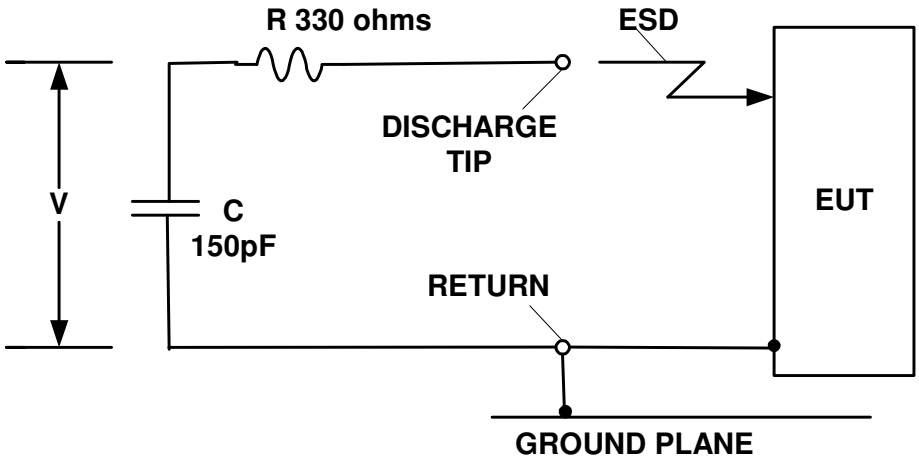
B. CONTRAST / RESPONSE TIME / VIEW ANGLE

WESTAR CORPORATION FPM-510



**Westar FPM-510
Display Contrast /
Response time /
View angle Analyzer**

C. ESD ON AIR DISCHARGE MODE



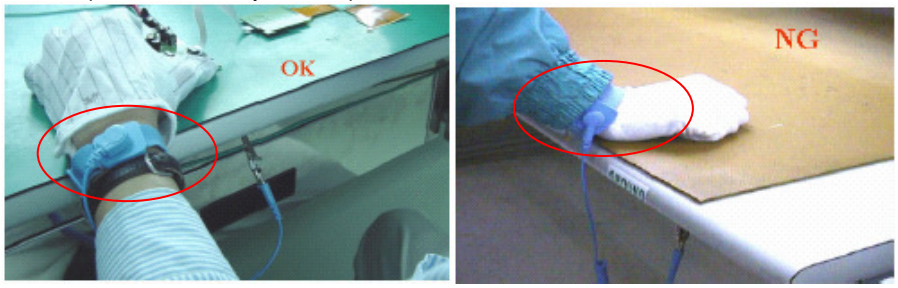
APPENDIX 3: PRECAUTIONS FOR USING THE OLED MODULE

Precautions for Handling

1. When handling the module, wear powder-free antistatic rubber finger cots, and be careful not to bend and twist it.

2. The OLED module is consisted of glass and film, and it should avoid pressure, strong impact, or being dropped from a high position.

3. The OLED module is an electronic component and is subject to damage caused by Electro Static Discharge (ESD). And hence normal ESD precautions must be taken when handling it. Also, appropriate ESD protective environment must be administered and maintained in the production line. When handling and assembling the panel, wear an antistatic wrist strap with the alligator clip attached to the ground to prevent ESD damage on the panel. Also, ground the tools being used for panel assembly and make sure the working environment is not too dry to cause ESD problems. Antistatic wrist strap should touch human body directly instead of gloves. (See below photos).



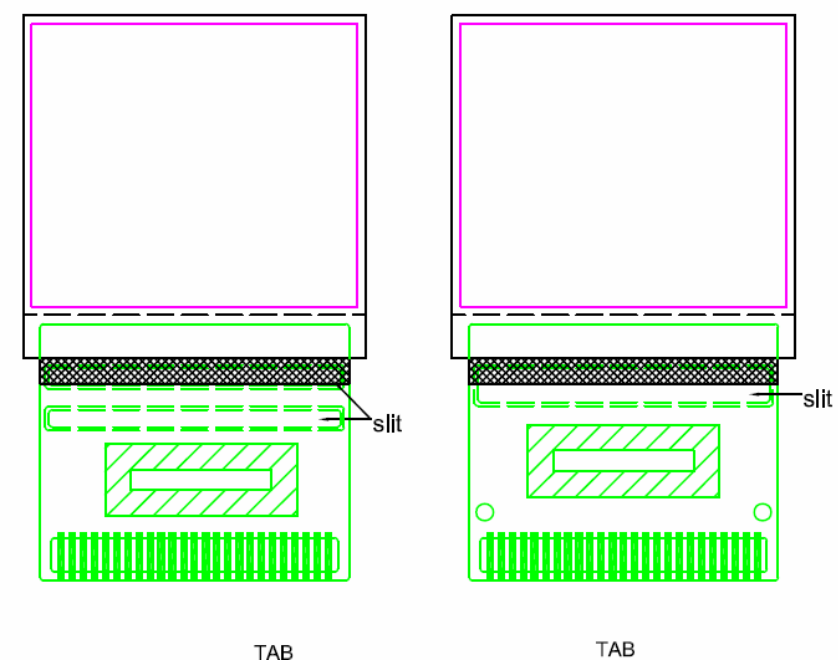
4. Take out the panel one by one from the holding trays for assembly, and never put the panel on top of another one to avoid the scratch.

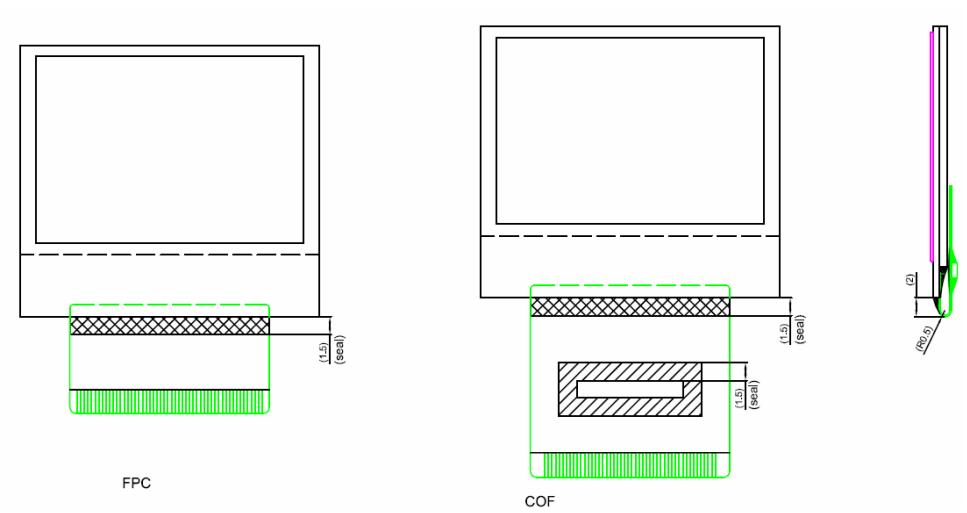
5. Avoid jerk and excessive bend on TAB/FPC/COF, and be careful not to let foreign matter or bezel damage the film.

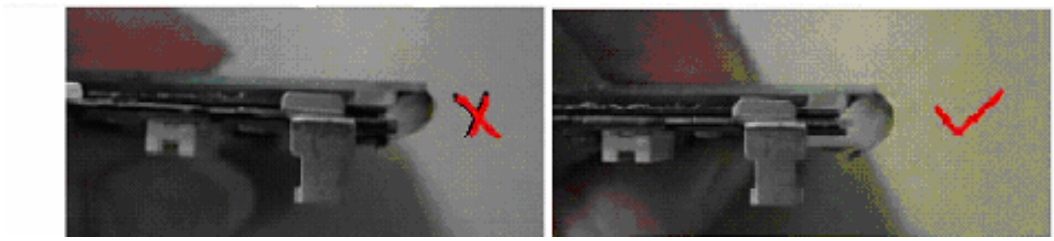
6. When handling and assembling the module (panel + IC), grab the panel, not the TAB/FPC/COF.

7. Use the tweezers to open the clicks on the connector of PCB before the insertion of FPC/COF, and click them back in. Once the FPC/COF sits properly in the connector, use the tweezers to avoid the damages.

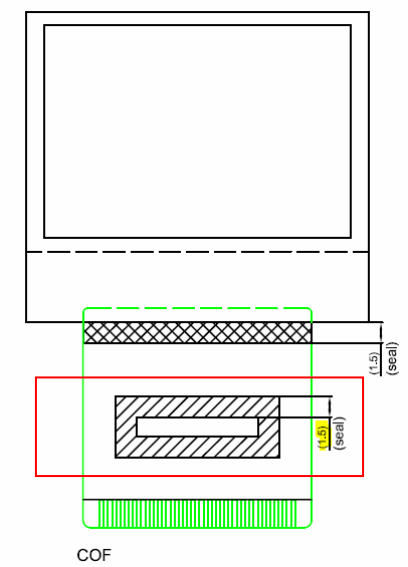
8. Please do not bend the film near the substrate glass. It could cause film peeling and TAB/FPC/COF damage. For TAB, It should bend the slit area as actual OLED it is. For FPC or COF, it is suggested to follow below pictures for instruction (distance between substrate glass and bending area >1.5mm; R>0.5mm).

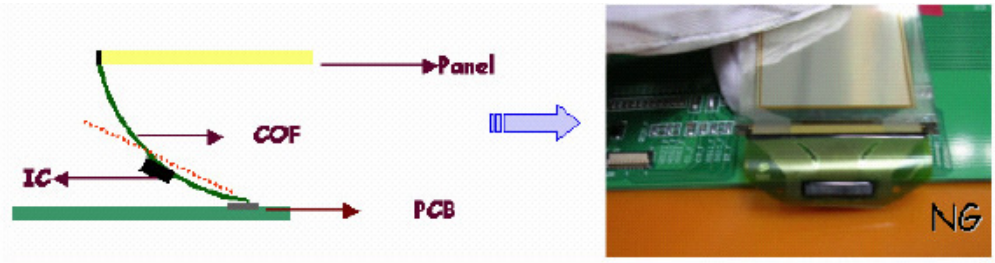




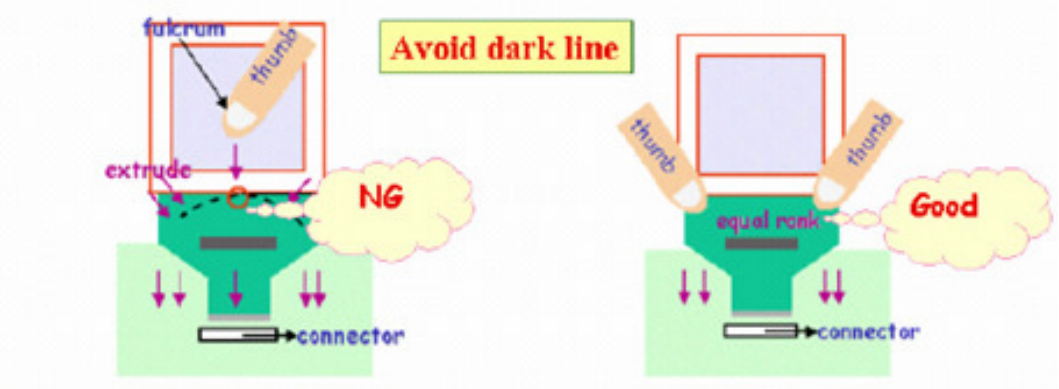


9. Avoid bending the film at IC bonding area. It could damage the IC ILB bonding. It should avoid bending the IC seal area. Please keep the bending distance >1.5mm.





10. Use both thumbs to insert COF into the connector when assembling the panel. Please refer to the photo.



11. The working area for the panel should be kept clean. If the panel is accidentally dropped on the floor, do visual inspection of the panel first. Please use clean-room wiping cloth moistened with alcohol to wipe it off if dirt or grease stains the panel.

12. Do not wipe the pin of film and polarizer with the dry or hard materials that will damage the surface. When cleaning the display surface, use the soft cloth with solvent, IPA or alcohol, to clean.

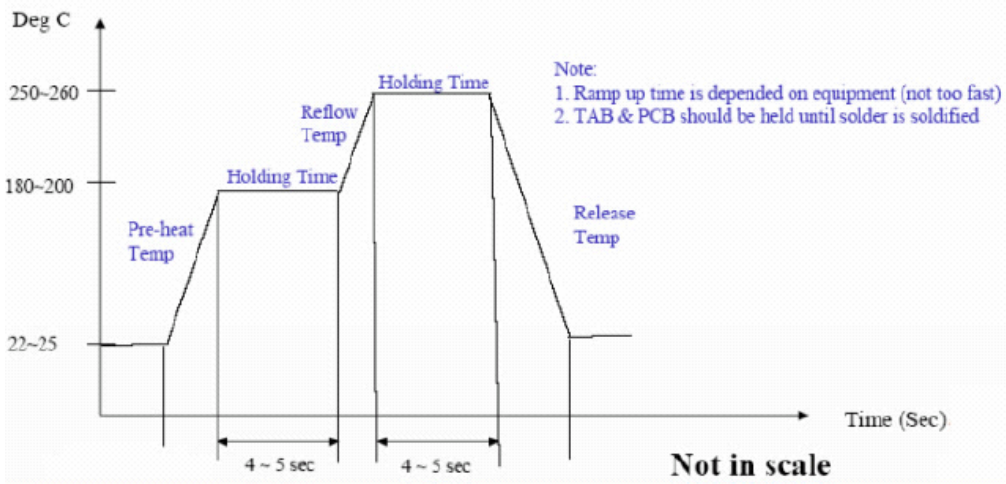
13. Protection film is applied to the surface of OLED panel to avoid the scratch. Please remove the protective film before assembling it. If the OLED panel has been stored for a long time, the residue adhesive material of the protective film may remain on the display surface after remove the protective film. Please use the soft cloth with solvent, IPA or alcohol, to clean.

14. When hand or hot-bar soldering TAB/FPC onto PCB, make sure the temperature and timing profiles to meet the requirements of soldering specification (the specification depends on the application or optimized by customer) to prevent the damage of IC pins by inappropriate soldering.

15. Solder residues arise from soldering process have to be cleaned up thoroughly before the module assembly.

16. Use the voltage and current settings listed in the specification to do the function test after the module assembly.

17. Suggestion for soldering process:
    i. TAB Lead- free soldering hot bar process
        1. Use pulse heated bonding tool equipment
        2. Material: Sn/Ag/Cu lead-free solder paste with typical 25um thickness on PCB pad. The TAB pin size and shape may be different, please base on the production line to adjust the thickness of PCB pad and temperature.
        3. Bonding Force:--4kg per centimeter square as the starting point.
        4. Suggested bonding tool temperature & time profile is as below for reference. Since there are differences in TAB soldering pins, soldering technicians' skills, mechanism…etc., the soldering conditions must be adequately tuned.



ii. TAB Lead- free soldering wire process
In case of manual soldering (Lead- free solder wire)
1. Solder wire contact iron directly: 280±5℃ at 3-5secs
2. Solder wire contact TAB lead directly (near iron but not contact): 380±5 ℃, 3-5secs
3. Since there are differences in TAB soldering pins, soldering technicians' skills, mechanism…etc., the soldering conditions must be adequately tuned.

iii. High temperature will result in rapid heat conduction to IC and might cause damage to IC, so please keep the temperature below 380 ℃. Also, avoid damaging the polyimide and solder resist which might take place at high temperatures. Refold cycles base on the de-soldering status, if the plating of pin was damaged, it can not be used again.

Precautions for Electrical

1. Design using the settings in the specification

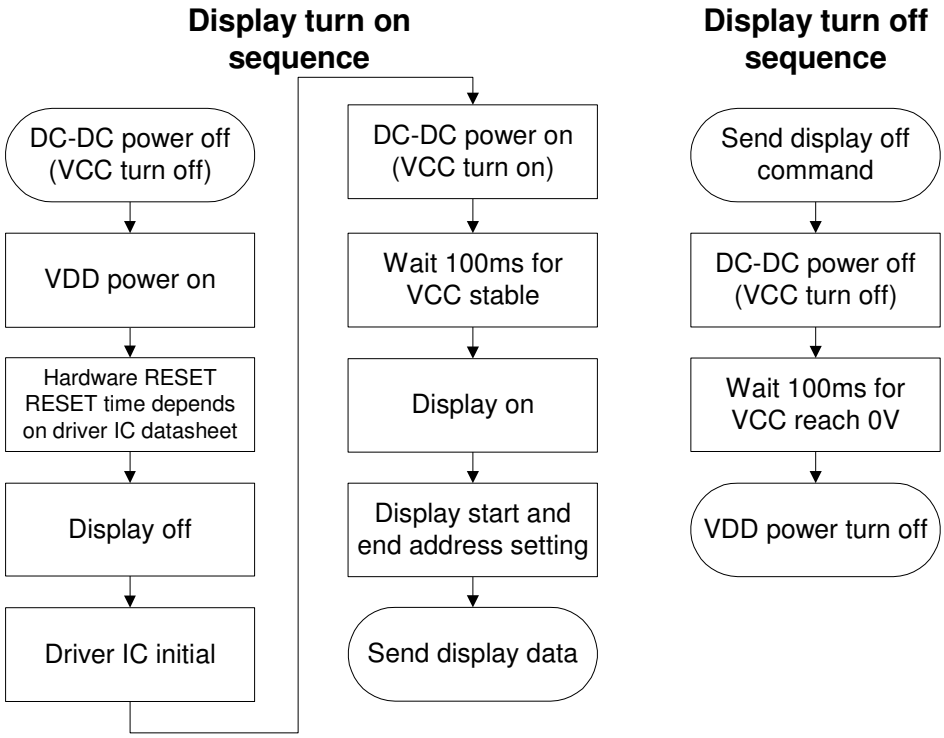
It is very important to design and operate the panel using the settings listed in the specification. It includes voltage, current, frame rate and duty cycle... etc. Operation the OLED outside the range of the specification should be entirely avoided to ensure proper operation of the OLED.

2. Maximum Ratings

To ensure the proper operation of the panel, never design the panel with parameters running over the maximum ratings listed in the specification. Also the logic voltages such as VIL and VIH have to be within the specified range in the specification to prevent any improper operation of the panel.

3. Power on/off procedure

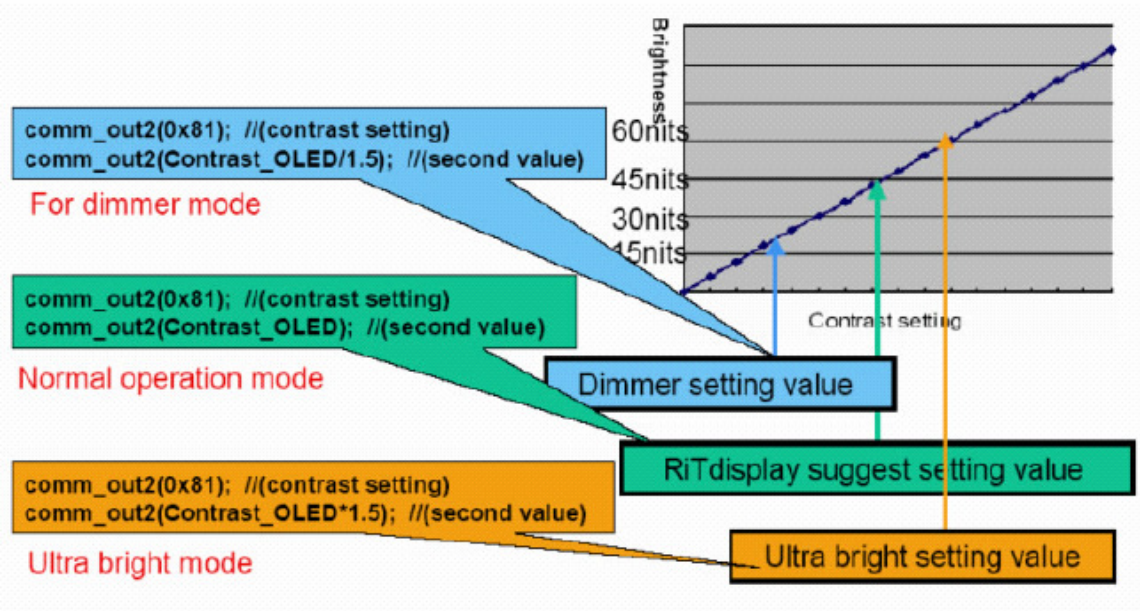
To avoid any inadvertent effects resulting from inappropriate power on/off operations, please follow the directions of power on/off procedure on page 6. Any operation that does not comply with the procedure could cause permanent damage of the IC and should be avoided. When the logic power is not on, do not activate any input signal. Abrupt shutdown of power to the module, while the OLED panel is on, would cause OLED panel malfunction.



4. Power savings

To save power consumption of the OLED, please use partial display or sleep mode when the panel is not fully activated. Also, if possible, make the black background to save power.

The OLED is a self-luminous device and a particular pixel cluster or image can be lit on via software control. So power savings can be achieved by partial display or dimming down the luminance. Depending on the application, the user can choose among Ultra Bright Mode, Normal Operation Mode, and Sleeping Mode. The power consumption is almost in directly proportion to the brightness of the panel, and also in directly proportion to the number of pixels lit on the panel. The customer can save the power by the use of black background and sleeping mode. One benefit from using these design schemes is the extension of the OLED lifetime.



5. Adjusting the luminance of the panel

Although there are a couple of ways to adjust the luminance of the panel, it is strongly recommended that the customer change the contrast setting to adjust the luminance of the panel. Adjusting voltages to achieve desired luminance is not allowed. Be aware that the adjustment of luminance would accompany the change of lifetime of the panel and its power consumption as well.

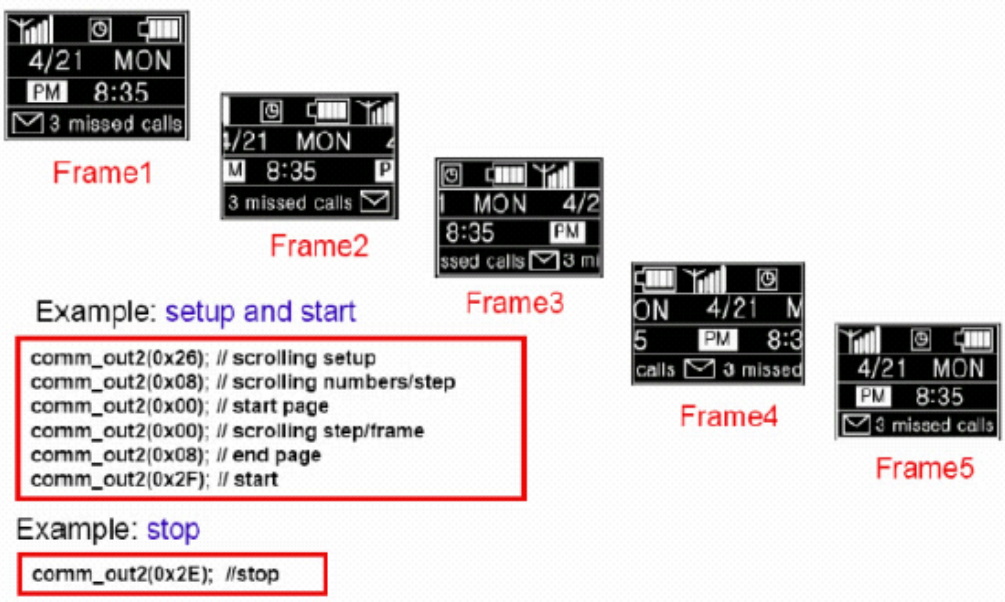
6. Residual Image (Image Sticking)

The OLED is a self-emissive device. As with other self-emissive device or displays consisting of self-emissive pixels, when a static image frozen for a long period of time is changed to another one with all-pixels-on background, residual image or image sticking is noticed by the human eye. Image sticking is due to the luminance difference or contrast between the pixels that were previously turned on and the pixels that are newly turned on. Image sticking depends on the luminance decay curve of the display. The slower the decay, the less prominent the image sticking is. It is strongly recommended that the user employ the following three strategies to minimize image sticking.

1. Employ image scrolling or animation to even out the lit-on time of each and every pixel on the display, also could use sleeping mode for reduced the residual image and extend the power capacity.
2. Minimize the use of all-pixels-on or full white background in their application because when the panel is turned on full white, the image sticking from previously shown patterns is the most revealing. Black background is the best for power savings, greatest visibility, eye appealing, and dazzling displays
3. If a static logo is used in the reliability test, change the pattern into its inverse (i.e., turn off the while pixels and turn on the previously unlit pixels) and freeze the inverse pattern as long as the original logo is used, so every pixel on the panel can be lit on for about the same time to minimize image sticking, caused by the differential turn-on time between the original and its reverse patterns.

Black Background

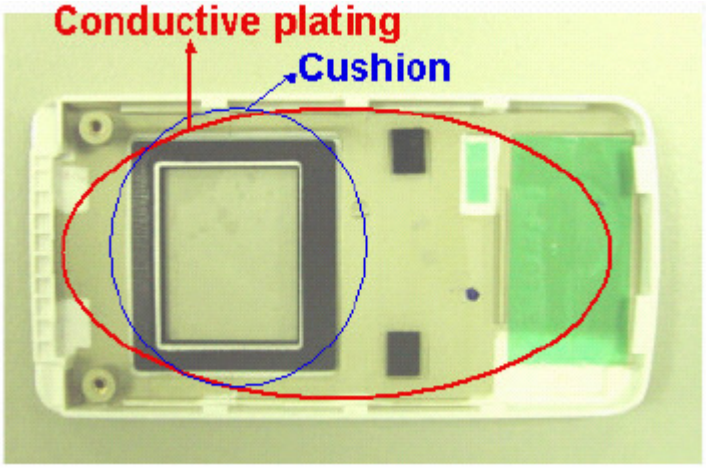
Scrolling example



Precautions for Mechanical

1. Cushion or Buffer tape on the cover glass

It is strongly recommended to have a cushion or buffer tape to apply on the panel backside and front side when assembling OLED panel into module to protect it from damage due to excessive extraneous forces.



It is recommended that a plating conductive layer be used in the housing for EMI/EMC protection. And, the enough space should be reserved for the IC placement if the IC thickness is thicker than the TAB film when customer design the PCB.

2. Avoid excessive bending of film when handling or designing the panel into the product

The bending of TAB/COF/FPC has to follow the precautions indicated in the specification, extra bending or excessive extraneous forces should be avoided to minimize the chances of film damage. If bending the film is necessary, please bend the designated bending area only. Please refer to items 8 and 9 of Precautions for Handling for more information.

Precautions for Storage and Reliability Test

1. Storage

Store the packed cartons or packages at 25℃±5℃, 55%±10%RH. Do not store the OLED module under direct sunlight or UV light. For best panel performance, unpack the cartons and start the production of the panels within six months after the reception of them.

2. Reliability Test

RiTdisplay only guarantees the reliability of the OLEDs under the test conditions and durations listed in the specification.